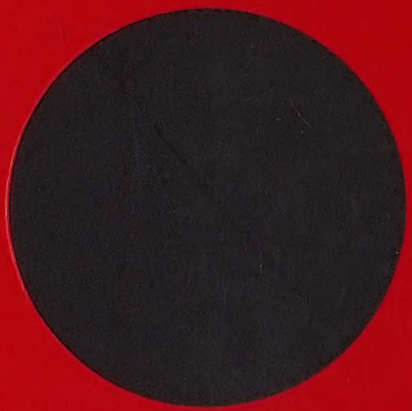
5500A

Ballantine



Ballantine

5500A

AUTOMETRONIC

COUNTER-TIMER

BALLANTINE LABORATORIES, INC.

P.O. BOX 97
BOONTON, NEW JERSEY 07005 USA
201-335-0900/TWX: 710-987-8380

901-0016-1A

JULY 1972

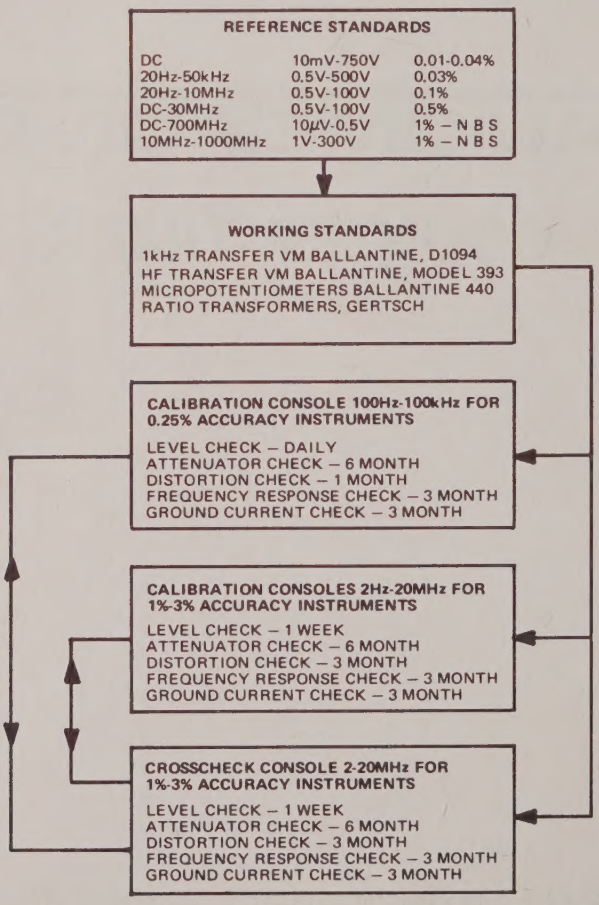
Printed in U.S.A.

WARRANTY

All Ballantine Laboratories, Inc. products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, except for vacuum tubes and batteries, or, in the case of certain major components listed in the instruction manual, for the specified period. We will repair or replace products which prove to be defective during the warranty period. No other warranty is expressed or implied. We are not liable for consequential damages.

CERTIFICATION

The equipment supplied on your order meets all applicable published Ballantine specifications as determined by thorough testing and inspection. Ballantine's calibration measurements are traceable to the National Bureau of Standards. All instruments used in calibrating Ballantine products are standardized by systematic reference to NBS-traceable standards as described in the validation procedures shown below.


REFERENCE STANDARDS
DC 10mV-750V 0.01-0.04%
20Hz-50kHz 0.5V-500V 0.03%
20Hz-10MHz 0.5V-100V 0.1%
DC-30MHz 0.5V-100V 0.5%
DC-700MHz 10μV-0.5V 1% – N B S
10MHz-1000MHz 1V-300V 1% – N B S
WORKING STANDARDS
1kHz TRANSFER VM BALLANTINE, D1094
HF TRANSFER VM BALLANTINE, MODEL 393
MICROPOTENTIOMETERS BALLANTINE 440
RATIO TRANSFORMERS, GERTSCH
CALIBRATION CONSOLE 100Hz-100kHz FOR 0.25% ACCURACY INSTRUMENTS
LEVEL CHECK – DAILY
ATTENUATOR CHECK – 6 MONTH
DISTORTION CHECK – 1 MONTH
FREQUENCY RESPONSE CHECK – 3 MONTH
GROUND CURRENT CHECK – 3 MONTH
CALIBRATION CONSOLES 2Hz-20MHz FOR 1%-3% ACCURACY INSTRUMENTS
LEVEL CHECK – 1 WEEK
ATTENUATOR CHECK – 6 MONTH
DISTORTION CHECK – 3 MONTH
FREQUENCY RESPONSE CHECK – 3 MONTH
GROUND CURRENT CHECK – 3 MONTH
CROSSCHECK CONSOLE 2-20MHz FOR 1%-3% ACCURACY INSTRUMENTS
LEVEL CHECK – 1 WEEK
ATTENUATOR CHECK – 6 MONTH
DISTORTION CHECK – 3 MONTH
FREQUENCY RESPONSE CHECK – 3 MONTH
GROUND CURRENT CHECK – 3 MONTH

Ballantine's Quality Assurance program satisfied the requirements of MIL-Q-9858.

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Notes

General Information

The Ballantine Autometronic Counter-Timer 5500A is a compact and lightweight instrument for precise frequency and time measurements. It contains a unique autoranging circuit (patent pending) that enables time and frequency measurements to be made without the need for any operator adjustments.

To familiarize the operator with the automatic operation of the 5500A, the following short description will describe the operation of a conventional, manually operated Counter-Timer, explain the difficulties involved in measuring frequency and time, and indicate how the problems are solved in the 5500A.

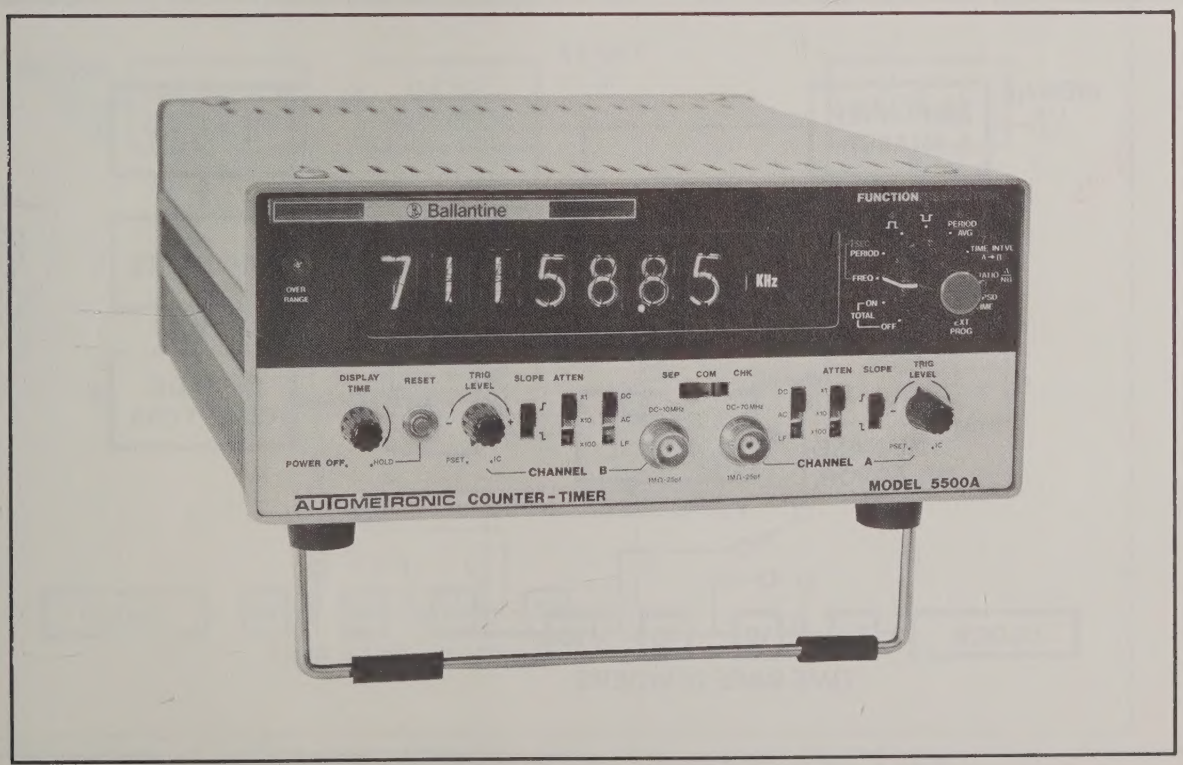


Figure 1-1. 5500A Autometronic Counter-Timer

FREQUENCY MEASUREMENTS:

In a conventional, manually operated electronic Counter-Timer, frequency measurements are performed as follows (see figure 1-2).

The input signal is amplified and shaped (1) in order to present pulses of uniform amplitude and rise time to the decade counters (5), regardless of the frequency or waveform of the input signal. The signal gate (4) controls the flow of the shaped pulses to the decade counters. When the signal gate is enabled (opened) by a pulse from the time base dividers (3) the shaped pulses pass through and are counted by the decade counters. The next pulse from the time base chain disables (closes) the gate. The count accumulated in the decade counters is decoded (6) to convert the information into useful signals to operate the display (7). The open gate interval is usually available in decade steps, derived from the basic clock period.

With conventional frequency counters, the operator must adjust the gate time selector (time base) and make measurements at several time base frequencies until maximum resolution is seen on the readout. This method of time base selection increases the measurement time, and complicates the design of systems incorporating frequency counters. Where signals of wide frequency range are to be measured, measurements are made very difficult, if not impossible.

The Autoranging feature enables the 5500A to overcome all the disadvantages of manual time base selection. The Autoranging circuitry automatically adjusts the time base of the instrument such that:

a. The display capacity is never exceeded.
b. The best possible resolution is always obtained, automatically.
c. Units of measurement (KHz, MHz) are automatically displayed.
d. The decimal point is computed and automatically placed in its correct position.

The automatic time base selection operation is concurrent with the measurement process. Thus maximum resolution is automatically obtained and needs no attention by the operator, or additional programming operations in an automatic measuring system. This increases measurement speed and simplifies system design. Signals of wide frequency range are immediately computed and displayed with maximum resolution.

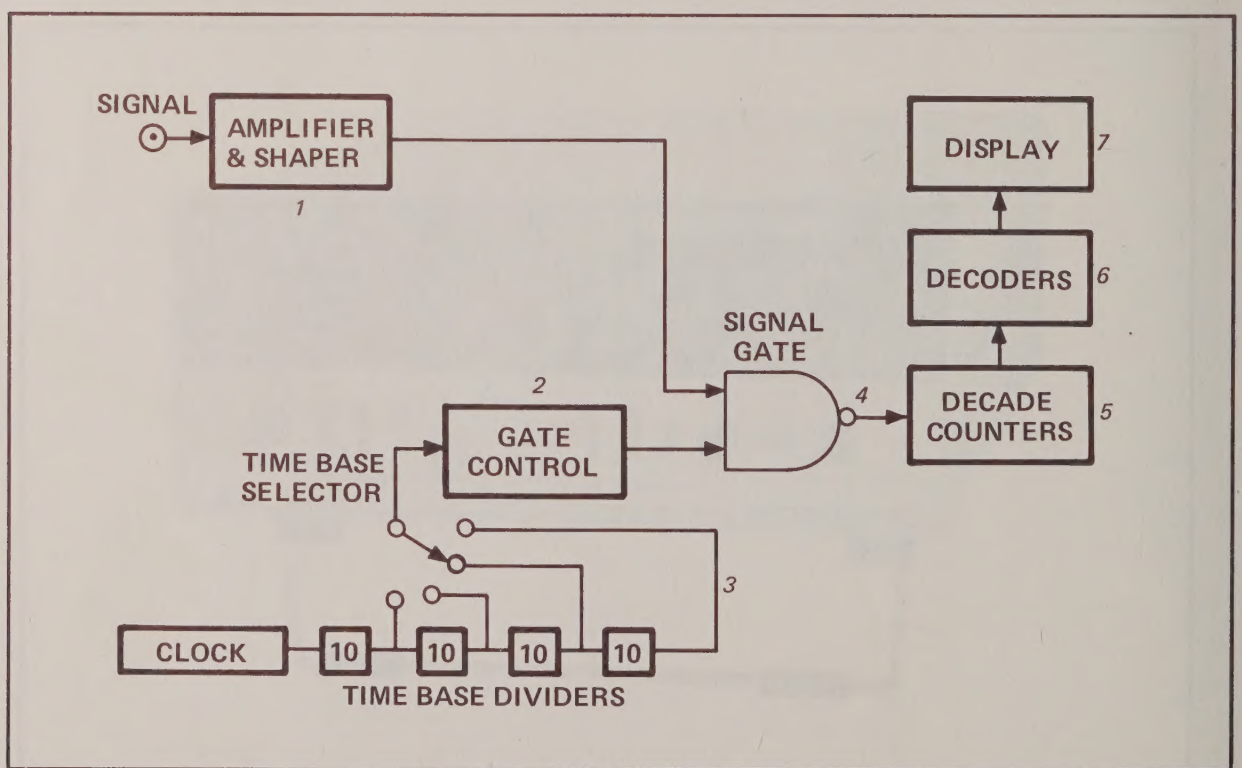


Figure 1-2. Conventional Frequency Counter Block Diagram

PERIOD AND TIME INTERVAL MEASUREMENTS:

In a conventional, manually operated electronic Counter-Timer, period or time interval measurements are performed as follows (see figure 1-3).

The input signal is applied to the amplifier and shaper (1) which converts the input signal to pulses of uniform amplitude and rise time. The shaped input signal operates a gate control circuit (2) which produces a gating pulse for the signal gate (4), equal in time to the period of the input signal. While the signal gate is enabled (open), pulses from the time base (3) pass through the signal gate to the decade counters (5). After the signal gate is closed, the count accumulated in the decade counters is decoded (6) to convert the information into useful signals to operate the display (7).

The difficulty in measuring period and time interval with the conventional method is that the operator has to know in advance the approximate duration of the signal in order to select a suitable time base (range) which will give the required resolution and prevent display overflow. If the input signal is repetitive, the operator will try to select manually, by making a few measurements, a suitable time unit for best results. However, if the input signal is non-repetitive or the time interval to be measured is of random duration, measurements are made very difficult, if not impossible.

The Autoranging feature enables the 5500A to overcome all the disadvantages of manual time base selection. The Autoranging circuitry automatically adjusts the time base units such that:

a. The display capacity is never exceeded, except for impracticably long periods ($K - 10^n$ seconds, where K is the lowest time unit and n the number of digits of the counter).
b. The best possible resolution is always obtained, automatically.
c. Units of measurement (microseconds, milliseconds or seconds) are automatically displayed.
d. The decimal point is computed and automatically placed in its correct position.

The automatic time base selection operation is concurrent with the measurement process, so that signals of random duration or duration changes are immediately computed and displayed with maximum resolution.

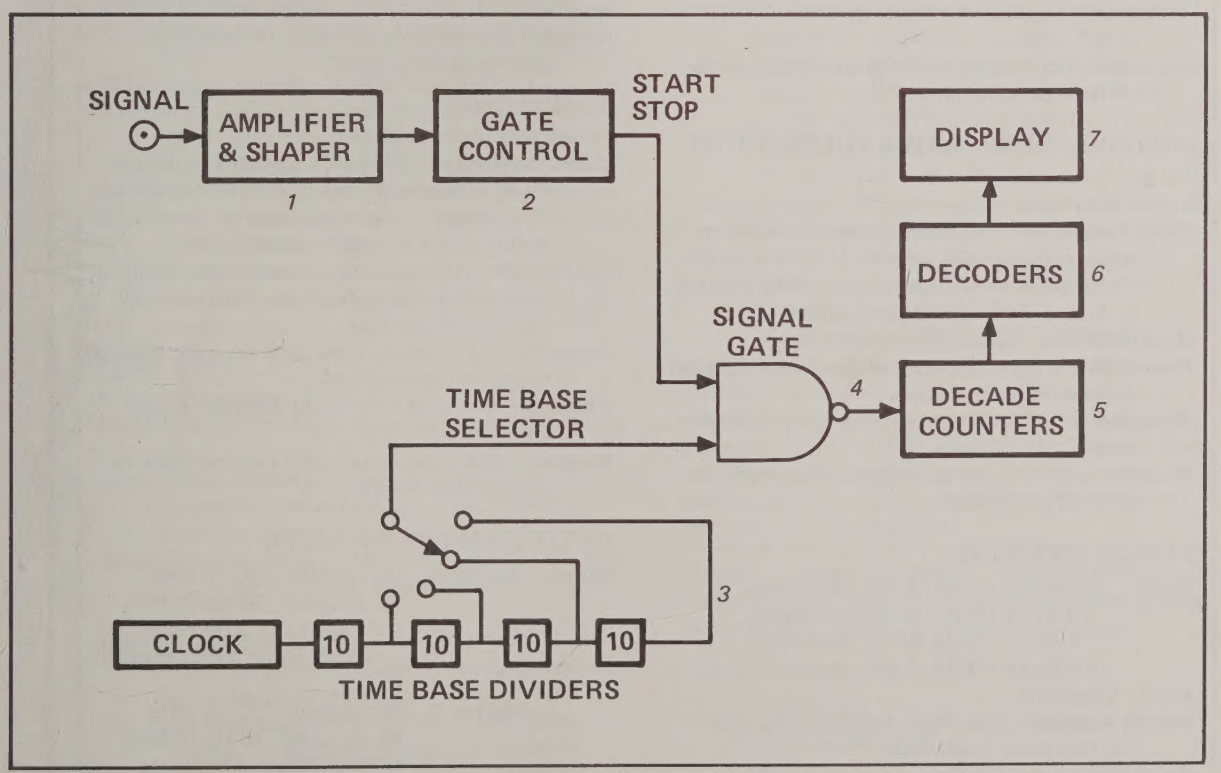


Figure 1-3. Conventional Period and Time Interval Meter Block Diagram

Table 1-1. Specifications

COUNT

Frequency: 0-70 MHz.
Counter Range: 1 to 10^7 counts.
Input: Channel A.
Gate Time: Manually selected.
Accuracy: Absolute.
Readout: Dimensionless.

FREQUENCY

Range: 0-70 MHz.
Input: Channel A.
Gate Time: Automatically selected to fill the display (up to 1 sec), or 1 sec manual. The number of digits displayed can be selected as 4, 5, or 7 by a front-panel switch.
Accuracy: ±1 count ± time-base accuracy.
Readout: kHz or MHz, with automatically positioned decimal point.

PERIOD

Range: 100 nsec to 10^7 seconds.
Input: Channel A.
Clock Frequency: 100 nsec to 1 second in decimal steps, automatically selected to fill the display. The number of digits displayed can be selected as 4, 5, or 7 by a front-panel switch.
Resolution: 0.1 μsec to 1 sec, automatically selected for maximum resolution.
Accuracy: ±1 count ± time-base accuracy ± trigger error*.
Readout: μsec, msec or sec, with automatically positioned decimal point.

POSITIVE OR NEGATIVE PULSE WIDTH

Range: 0.1 μsec to 10^7 sec.
Input: Channel A.
Clock Frequency: 100 nsec to 1 second in decimal steps, automatically selected to fill the display. The number of digits displayed can be selected as 4, 5, or 7 by a front-panel switch.
Slope Selection: Automatically selected.
Resolution: 0.1 μsec to 1 sec, automatically selected for maximum resolution.
Accuracy: ±1 count ± time-base accuracy ± trigger error*.
Readout: μsec, msec or sec, with automatically positioned decimal point.

PERIOD AVERAGE

Range: 100 Hz to 1 MHz, 4-digit resolution.
10 Hz to 1 MHz, 5-digit resolution.
1 Hz to 1 MHz, 6-digit resolution.
0.1 Hz to 1 MHz, 7-digit resolution.
Input: Channel A.
Periods Averaged: 1 to 1000, automatically selected for maximum resolution.
Clock Frequency: 1 MHz.
Accuracy: ±1 count ± time-base accuracy ± trigger error*.
Readout: μsec, with automatically positioned decimal point.

TIME A→B

Range: 0.1 μsec to 10^7 sec.
Input: Start Signal: Channel A. Stop Signal: Channel B. Can be common or separate.
Clock Frequency: 100 nsec to 1 second in decimal steps, automatically selected to fill the display. The number of digits displayed can be selected as 4, 5, 6 or 7 by a front-panel switch.
Resolution: 0.1 μsec to 1 sec, automatically selected for maximum resolution.
Accuracy: ±1 count ± time-base accuracy ± trigger error of A* ± Trigger error of B*.
Readout: μsec, msec, or sec, with automatically positioned decimal point.

RATIO A/NB

Range: Channel A: 0-70 MHz. Channel B: 0-10 MHz.
Input (F1): Channel A.
Input (F2): Channel B.
Measures: F1/F2.
Number of Cycles of F2 Averaged: 1 to 1000 automatically selected for maximum resolution.
Accuracy: ±1 count of F1 ± trigger error of F2*.
Readout: Dimensionless, with automatically positioned decimal point.

TIME INTVL

Range: 0.1 μsec to 10^7 sec.
Clock Frequency: 100 nsec to 1 second in decimal steps, automatically selected to fill the display. The number of digits displayed can be selected as 4, 5, 6 or 7 by a front-panel switch.
Gate Signal: Via rear panel connector. Contact closure to ground or saturated transistor will control the gate time.
Resolution: 0.1 μsec to 1 sec, automatically selected for maximum resolution.
Accuracy: ±1 count ± time-base accuracy ± gate error.**
Readout: μsec, msec or sec, with automatically positioned decimal point.

INPUT CHANNELS A AND B

Range: Channel A, DC coupled: DC-70 MHz
AC coupled: 20 Hz-70 MHz
HF Rejection: Attenuates signals above 1 kHz approx.

Channel B, DC coupled: DC-10 MHz
AC coupled: 20 Hz-10 MHz
HF Rejection: Attenuates signals above 1 kHz approx.

Table 1-1. Specifications (Continued)

Impedance: 1 megohm shunted by 25 pF approx.
Sensitivity: 25 mV rms sine wave 0-2 MHz.
50 mV rms sine wave 2-10 MHz.
100 mV rms sine wave 10-70 MHz (channel A only).
Channel A, 0.3 V peak-to-peak pulse, 7 nsec min pulse width.
Channel B, 0.3 V peak-to-peak pulse, 50 nsec min pulse width.
Preset: Sets trigger reference to 0 volts.
Attenuation: X1, X10, X100.
Trigger Level: Continuously adjustable ±1 V, ±10 V, ±100 V, dependent upon setting of attenuator.
Slope: Independent selection of positive or negative slope.
Overload Protection: 250 V rms on X10 and X100 attenuator settings, 120 V rms on X1 attenuator setting up to 1 kHz, decreasing to 10 V rms above 10 MHz.
Shaped Outputs A and B: Terminals on the rear panel for external monitoring of the triggering points on the input signals. > 1 volt open circuit.

DISPLAY

Numerical: 6 digits (7 optional).
Units: kHz, MHz, μsec, msec or sec, automatically computed and displayed.
Decimal Point: Automatically selected.
Display Storage: Prior reading is held while new reading is being made. Display time is adjustable from 0.2 to 5 seconds or held indefinitely.
Gate: Lights up when counter gate is open.
Overrange: Solid-state indicator that lights up when the counter capacity is exceeded. Due to the automatic gate selection, the counter capacity can be exceeded only when using the manually selected 1 sec gate time in Frequency mode or in the Period Average and Ratio modes.
Manual Reset: Front-panel pushbutton switch resets the display and all registers, and initiates a new measurement.

TIME BASE

Crystal Frequency: 10 MHz
Crystal Oven: Self-regulating solid-state proportional oven.
Aging Rate: Less than 2 parts in 10^8 per day after 10 days of continuous operation. (less than 0.02 ppm per day)
Temperature Stability: Less than 2 parts in 10^6 from 0°C to +50°C. (Normally less than 0.04 ppm per °C)
Line Voltage Stability: Less than 5 parts in 10^7 for ±10% line voltage change. (Nominally less than 0.05 ppm per % change)
Ext. Time Base Input: Via rear panel BNC connector, 1 kHz to 10 MHz, 0.5 V rms into 1 Kohm.
Int. Time Base Output: 1 MHz via rear panel BNC connector.

GENERAL

Display: 6 gas discharge type numeric indicators (7 optional)
Operating Temperature: 0°C (+32°F) to +50°C (+122°F).
Power Requirements: 115 or 230 volts ±10%, 48 to 400 Hz, 25 watts.
Dimensions: 3 1/2" (88 mm) H x 8 3/8" (212 mm) W x 12 1/2" (316 mm) D.
Weight: 7 pounds (3.2 Kg).
Accessories Furnished: Power cord, Service Manual.

ACCESSORIES AVAILABLE

Probe Kit — Attenuator 10:1/1:1 6 ft., P/N 10601A
50 ohm 4 ft BNC-to-BNC coaxial cable, P/N 12249D
Display Extender Board, P/N 89400001A
6 ft cable to connect the 5500A to a digital recorder, 12253A
6 ft cable to connect the 5500A for remote programming, 12254A
Feed thru Termination, 50 ohm BNC, 12630A
50 ohm 4 ft BNC to alligator cable, 12250D

OPTIONS AVAILABLE

7-DIGIT DISPLAY (Option No. 07)
PRINTER OUTPUT (Option No. 01)
Logic: Positive True BCD & Dec. Pts., Units Negative True
Form: 4-line 1-2-4-8 BCD. "1" state level: +5 ±0.5V 2.5 Kohm source impedance nominal. "0" state level: +0.25 V at −1 mA.
Print Command: Positive pulse of 5 V, DC coupled. Source impedance is 5 Kohm when in the "high" state and 500 ohm when in the "low" state. Pulse duration is 1 msec approx. Occurs at end of gate time.
Inhibit Input: A positive pulse of 3 V minimum and 50 V maximum will inhibit the recycling circuitry of the counter.
Connector: Amphenol 57—40500 (50-pin blue ribbon). Mating connector Amphenol 57—30500. P/N 31100500A

REMOTE PROGRAMMING (Option No. 02)
Permits function and resolution to be remotely selected by a single contact to ground or equivalent active circuit. (TTL & DTL compatible) The time base is automatically selected for maximum resolution. Mating connector (24-pin Blue Ribbon) Amphenol 57-30240, P/N 31100370A

*Trigger error is less than 0.3% of one period divided by the number of periods averaged, for signals with a signal-to-noise ratio of 40 db or better, and 100 mV rms amplitude.

**For any waveshape, trigger error is less than

$$\frac{0.0025}{\pm \text{Signal slope (Volts/}\mu\text{s)}}$$ Microseconds.

Table 2-1. REMOTE PROG Connector

NOTE: When Remote Programming Option 02 is not part of the instrument, the 24-pin connector is replaced by banana jacks. The red banana jack is the TIME INTERVAL input; the black banana jack is ground. (See Figure 4-9).

PIN	USE	PIN	USE
1	Common	13	5 Digit Resolution
2	Count Start	14	6 Digit Resolution
3	Freq	15	7 Digit Resolution
4	Period	16	
5	Positive Pulsewidth	17	
6	Negative Pulsewidth	18	
7	Period Avg	19	
8	Time A→B	20	
9	A/NB	21	
10	Time Intvl	22	Reset
11	1 Sec Timebase	23	Time Intvl Enable
12	4 Digit Resolution	24	GND

Table 2-2. PRINTER Connector

PIN	USE	PIN	USE
1	10^0 Decade BCD 1 Output	26	10^0 Decade BCD 4 Output
2	10^0 Decade BCD 2 Output	27	10^0 Decade BCD 8 Output
3	10^1 Decade BCD 1 Output	28	10^1 Decade BCD 4 Output
4	10^1 Decade BCD 2 Output	29	10^1 Decade BCD 8 Output
5	10^2 Decade BCD 1 Output	30	10^2 Decade BCD 4 Output
6	10^2 Decade BCD 2 Output	31	10^2 Decade BCD 8 Output
7	10^3 Decade BCD 1 Output	32	10^3 Decade BCD 4 Output
8	10^3 Decade BCD 2 Output	33	10^3 Decade BCD 8 Output
9	10^4 Decade BCD 1 Output	34	10^4 Decade BCD 4 Output
10	10^4 Decade BCD 2 Output	35	10^4 Decade BCD 8 Output
11	10^5 Decade BCD 1 Output	36	10^5 Decade BCD 4 Output
12	10^5 Decade BCD 2 Output	37	10^5 Decade BCD 8 Output
13	10^6 Decade BCD 1 Output	38	10^6 Decade BCD 4 Output
14	10^6 Decade BCD 2 Output	39	10^6 Decade BCD 8 Output
15		40	
16		41	
17	μsec*	42	Sec*
18	msec*	43	
19	Decimal Point 1 (right-most)	44	Decimal Point 2
20		45	Decimal Point 3
21	KHz*	46	MHz*
22	Inhibit Input	47	
23	Positive Print Command	48	
24		49	
25		50	Ground

*Units provide negative logic.

Installation

2-1. INTRODUCTION

The 5500A is shipped in an operating condition and is essentially ready for use as received. This section contains unpacking, inspection, and installation information.

2-2. UNPACKING AND INSPECTION

Examine the shipping carton for damage before unpacking the instrument. Carefully remove the instrument from the carton. Check immediately for loose or broken control knobs, bent or broken connectors, and damage to any cabinet part. If damage of any nature is found, refer to the warranty instructions.

2-3. POWER CONNECTION CAUTION

This instrument is designed to operate from either a 115 vac or 230 vac power source. The primary voltage selection is made by positioning a recessed slide switch on the rear panel. To change the position of the slide switch, insert a small screwdriver in the switch slot and set the switch to the required voltage position. Damage caused by using incorrect primary input voltage voids the instrument warranty.

WARNING

The instrument is provided with a three-conductor power cord which will ground the case when connected to a three-connector grounding outlet. If a grounding outlet is not available, an adapter must be used which provides a good grounding connection.

2-4. COOLING

Cooling air enters the case through holes on the covers. Adequate clearance must be provided on all sides of the instrument to allow heat to be dissipated. Be sure that the instrument position permits adequate air circulation and that nearby equipment does not discharge hot air directly on the instrument.

2-5. REMOTE PROGRAMMING

The REMOTE PROGRAMMING connector on the rear panel is an optional feature which permits remote programming of the instrument. Table 2-1 lists each of the pins in this connector and the corresponding function. Note that instrument functions can only be remotely programmed when the front panel FUNCTION/RESOLUTION switch is set to REMOTE PROGRAMMING. When the Remote Programming option is not required, two binding posts are installed, which provide a remote enable input to the instrument in the TIME INTVL mode. A logic "O" applied to the binding posts enables the internal gate and a logic "1" disables it.

The front panel controls that are programmable are the FUNCTION and RESOLUTION switches. The controls which are not programmable are: DISPLAY TIME, SEP-COM-CHK and CHANNEL A and CHANNEL B controls. Selection of remote programming is made by setting the FUNCTION switch to REMOTE PROGRAMMING. This provides a ground potential to pin 1 of the REMOTE PROGRAMMING connector. This ground can be used as an enabling level for the remote programming unit.

All lines may be controlled by TTL or DTL signals or contact closure to ground.

NOTE

When the unit is NOT being programmed, all the lines should be left open or pulled to +5 V by not less than 2 kohm.

2-6. DIGITAL RECORDER

The PRINTER connector on the rear panel is an optional feature which provides BCD outputs and control signals for operating a digital recorder. Table 2-2 lists each of the pins in the connector. The characteristics of each input and output are given in the data sheet in front of this manual.

2-7. CLOCK SELECTION

An internal 10 MHz clock is provided. There is also provision for using an external clock for increased stability or to obtain a special time base. The clock selection is made by positioning of the rear panel two-position recessed slide switch INT-EXT CLOCK to INT when using the internally provided clock, and to EXT when applying an external clock.

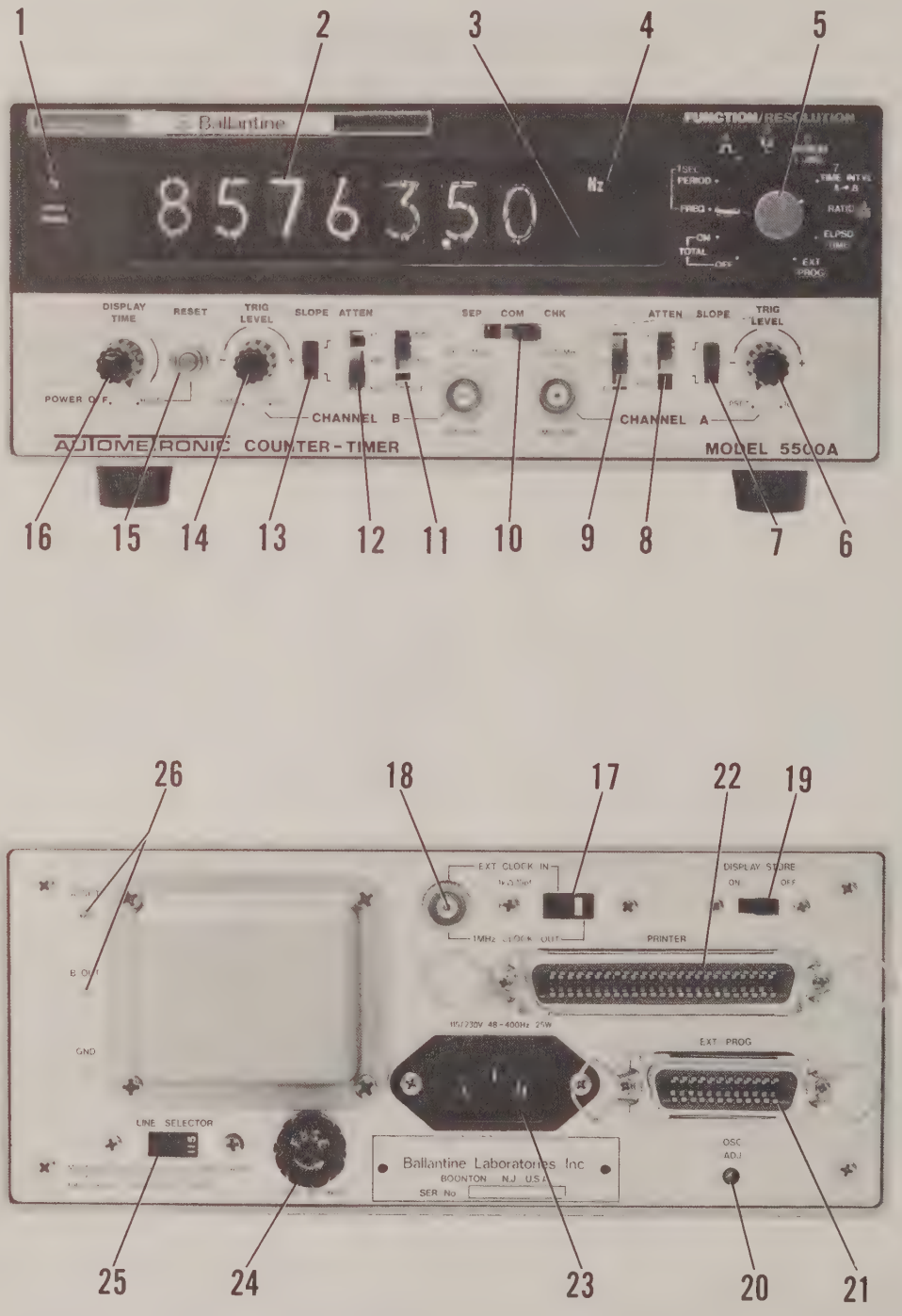


Figure 3-1. Controls, Connectors and Indicators

Section 3

Operation

3-1. INTRODUCTION

This section will familiarize the operator with the typical operation procedures of the 5500A. The front and rear panel controls, connectors, and indicators are described. Recommended operating procedures demonstrate instrument flexibility.

3-2. CONTROLS, CONNECTORS, INDICATORS

Figure 3-1 shows the instrument's front and rear panel and table 3-1 describes the function of the element located there. These descriptions are not intended to be operating instructions but, briefly, to familiarize the operator with the instrument.

Table 3-1. Controls, Connectors and Indicators

INDEX NO	ITEM	FUNCTION
1	OVER RANGE Indicator	A light emitting diode that lights up when the display range of the instrument has been exceeded.
2	Display	A six-digit (seven digit optional) numeric readout with automatically positioned decimal point that indicates the magnitude of the quantity measured. The units for the readout are shown by indicators to the right of the display (μsec, msec, sec, KHz, and MHz).
3	GATE Indicator	Indicator lamp that lights up when the instrument is counting.
4	μsec, msec, sec, KHz, MHz Indicators Indicators	Indicator lamps to show the units of the readout.
5	FUNCTION/RESOLUTION Switch	A dual concentric switch assembly. Used to select the mode of operation and the number of digits to be displayed (resolution)
6	Channel A TRIGGER LEVEL	A potentiometer that varies the triggering level of the input waveform. A preset trigger level suitable for symmetrical-to-ground waveforms is obtained when the control is set to PSET (fully counter-clockwise).
7	Channel A SLOPE Switch	A two-position slide switch that permits triggering on either positive or negative edges of a signal supplied to Channel A in the PERIOD, PERIOD AVG and TIME A-B modes. In all other modes, the slope selection is internal.
8	Channel A ATTEN Switch	A three-position slide switch that varies the attenuation (X1, X10, X100) of the signal applied to the Channel A connector.
9	Channel A Coupling Selector	A three-position slide switch that selects the coupling (AC or DC) or attenuates signals above 1 KHz (LF).
10	SEP-COM-CHK Switch	A three-position slide switch that connects Channel A and Channel B input circuits to a common input connector (Input A) or to separate connectors. In the position CHK (check) the internal 1 MHz oscillator is applied simultaneously to both channels.

Continued on next page

Table 3-1. Controls, Connectors and Indicators (Continued)

11	Channel B Coupling Selector	Similiar to Channel A Coupling Selector
12	Channel B ATTEN Switch	Similiar to Channel A ATTEN Switch
13	Channel B SLOPE Switch	Similiar to Channel A SLOPE
14	Channel B TRIGGER LEVEL Control	Similiar to Channel A TRIGGER LEVEL Control
15	RESET Pushbutton	Resets display and internal count to zero and starts a new measurement.
16	DISPLAY TIME Control	A switch/potentiometer control that applies ac power to the instrument, and controls the display time.
17	INT-EXT CLOCK Switch	A recessed two-position slide switch that permits selection of either the internal clock or an external clock. When set to INT, a 1 MHz signal derived from the internal clock is available to the 1 MHz CLOCK OUT BNC Connector.
18	Clock In-Out Connector	A BNC connector that enables either the application of an external clock to the instrument or provision of the internal clock from the instrument.
19	STORAGE Switch	A two-position slide switch. When set to ON, provides display storage while new measurement is being made. In OFF position, allows continous display.
20	OSC ADJ	A trimmer capacitor used for oscillator adjustment.
21	REMOTE PROG Connector	A 24-pin connector for remote programming signals to the instrument.
22	PRINTER Connector	A 50-pin connector for digital recorder interconnection.
23	AC Power Connector	IEC type with offset pin connected to instrument chassis.
24	Fuse	Protects primary power circuit from accidental overload.
25	LINE SELECTOR Switch	Selects the nominal line voltage to operate the instrument.
26	A OUT, B OUT Terminals	Used for monitoring of the triggering points on the input signals.

3-3. GENERAL OPERATING INFORMATION

The 5500A has ten operating modes and a test mode. The operating modes are: COUNT, FREQ, PERIOD, POSITIVE PULSEWIDTH, NEGATIVE PULSEWIDTH, PERIOD AVERAGE, TIME A→B, RATIO A/NB, TIME INTVL and REMOTE PROG. The REMOTE PROGRAMMING Mode permits remote operation of any of the instrument functions except the test mode. The following is a description of each operating mode and a typical application for each. The test mode is described in paragraph 3-5.

COUNT MODE:

In the count mode, the total number of pulses applied to the channel a jack in the interval determined locally by the FUNCTION/RESOLUTION switch is displayed. Input pulses may be of any shape and duty cycle, and may be applied either at random or a constant repetition rate. The count mode can be used to measure quantities or rates. For example, if a transducer is used to generate a pulse for each person boarding a bus, the total number of people on the bus is counted.

The count mode can also be used for totalizing, because disabling counting does not reset the instrument, unless the RESET button is pressed, the count is retained in storage. Thus, if the instrument is not reset, and counting is reenabled, the new count will add to the stored count and the display will indicate the total of the two individual counts.

FREQ MODE:

In the FREQ mode, the average frequency of a signal applied to the CHANNEL A jack is measured. This is done by counting the input pulses over an interval determined by the internal time base. The time base is automatically varied to provide the maximum resolution for the applied signal. The maximum number of digits displayed is variable from 4 to 6 (4 to 7 optional) by the FUNCTION/RESOLUTION switch. Table 3-2 lists the positions of this switch and gives the corresponding readouts for a range of input frequencies.

PERIOD MODE:

In the PERIOD Mode, the period of a signal applied to the CHANNEL A jack is measured. This is done by counting the pulses produced by the internal time base over a single period of the input signal. The time base is automatically varied to provide the maximum resolution for the applied signal. The maximum number of digits displayed is variable from 4 to 6 (4 to 7 optional) by the FUNCTION/RESOLUTION switch. Table 3-3 lists the positions of this switch and gives the corresponding readouts for a range of input frequencies.

POSITIVE PULSEWIDTH AND NEGATIVE PULSEWIDTH MODES:

In the POSITIVE PULSEWIDTH and NEGATIVE PULSEWIDTH Modes, the pulses produced by the internal time base are counted over the period of the input signal.

PERIOD AVERAGE MODE:

In the PERIOD AVERAGE Mode, the average period of a signal applied to the CHANNEL A jack is measured. This is done by counting the pulses produced by the internal time base over from 1 to 10^3 periods of the input signal. The number of periods over which the frequency is averaged, is automatically selected to provide maximum resolution for the applied signal. Table 3-4 gives the 7-digit display readout, and the number of periods over which the frequency is averaged, for a range of input frequencies

TIME A→B MODE:

In the TIME A→B Mode, the pulses produced by the internal time base are counted over the interval between the supply of a start pulse to the INPUT A jack and the supply of a stop pulse to the INPUT B jack. One application for the TIME A→B Mode is the measurement of elapsed time between two signals. The TIME A→B Mode can also be used to measure the elapsed time between two selected points on a single waveform.

RATIO A/NB MODE:

In the RATIO A/NB Mode, the ratio of two frequencies can be measured. The source of one frequency is applied to the CHANNEL A jack and the source of the other frequency is applied to the CHANNEL B jack. Both jacks are located on the front panel. The measurement is made by counting the number of A pulses occuring in 1 to 10^3 periods of B. The number of periods over which the A pulses are counted is automatically selected to provide maximum resolution. This gives a readout of the ratio of frequency A to frequency B with automatic positioning of the decimal point. The frequency limits of the A and B inputs must be observed.

TIME-INTVL MODE:

In the TIME-INTVL Mode, the pulses produced by the internal time base are counted over the interval determined by the remote Count-Enable input. Counting is enabled when the input is a logic 0 and is inhibited when the input is a logic 1. Thus, if a square wave (varying between the logic levels) is applied to the Count-Enable input, the instrument indicates half the period of the waveform. Resetting is not automatic in the TIME-INTVL Mode. Unless the instrument is reset manually, the value obtained in the first interval will be stored and will add to the count obtained is subsequent intervals.

One application for the TIME-INTVL Mode is the measurement of elapsed time, where the Count-Enable input is switched to a logic 0 at the start of the interval and then switched back to a logic 1 at the end of the interval. Other applications include measurements of pulsewidth, duty cycle and time A to B where A and B are separate start/stop times.

REMOTE PROGRAMMING MODE:

In the REMOTE PROGRAMMING Mode, all functions may be remotely selected through pins on the optional rear-panel REMOTE PROG connector. The connector pin used for each function is given in Table 2-1.

Table 3-2. Frequency Measurement Data

INPUT FREQUENCY	SWITCH POSITION 4	5	6	7
10 MHz	10.00 MHz	10.000 MHz	10000.0 KHz	10000.00 KHz
1 MHz	1.000 MHz	1000.0 KHz	1000.00 KHz	1000.000 KHz
100 KHz	100.0 KHz	100.00 KHz	100.000 KHz	0100.000 KHz
10 KHz	10.00 KHz	10.000 KHz	010.000 KHz	0100.000 KHz
1 KHz	1.000 KHz	01.000 KHz	001.000 KHz	0001.000 KHz
100 Hz	0.100 KHz	00.100 KHz	000.100 KHz	0000.100 KHz
10 Hz	0.010 KHz	00.010 KHz	000.010 KHz	0000.010 KHz

Table 3-3. Period Measurement Data

PERIOD OF INPUT SIGNAL	SWITCH POSITION 4	5	6	7
10 sec	10.00 sec	10.000 sec	10000.0 msec	10000.00 msec
1 sec	1.000 sec	1000.0 msec	1000.00 msec	1000.000 msec
100 msec	100.0 msec	100.00 msec	100.000 msec	100000.0 μsec
10 msec	10.00 msec	10.000 msec	10000.0 μsec	010000.0 μsec
1 msec	1.000 msec	1000.0 μsec	0100.0 μsec	001000.0 μsec
100 μsec	100.0 μsec	0100.0 μsec	00100.0 μsec	000100.0 μsec
10 μsec	010.0 μsec	0010.0 μsec	00010.0 μsec	000010.0 μsec
1 μsec	001.0 μsec	0001.0 μsec	00001.0 μsec	000001.0 μsec

Table 3-4. Period Average Measurement Data

PERIOD OF INPUT SIGNAL	NO. OF PERIODS AVERAGED	READOUT
1 sec	1	1000000 μsec
100 msec	10	100000.0 μsec
10 msec	100	10000.00 μsec
1 msec	1000	1000.000 μsec
100 μsec	1000	0100.000 μsec
10 μsec	1000	0010.000 μsec
1 μsec	1000	0001.000 μsec

3-4. INPUT CIRCUIT ADJUSTMENT

The input controls for both the A Channel and the B Channel are identical. The correct setting of these controls is of prime importance in order to obtain the best possible results.

The choice of ac or dc coupling depends on the type of signal to be measured. If the signal has a small ac component riding on a dc level, ac coupling should be used. For symmetrical signals, ac coupling is desirable. For very assymetrical signals like pulses with low duty cycle, dc coupling is preferable, particularly if the pulses are random. For waveforms below 1 KHz, the coupling selector switch should be set to HF REJ. This position attenuates signals above 1 KHz and will filter out noise superimposed on the input waveform.

Attenuation should be selected as required: X1 (±1 volt), X10 (±10 volts) or X100 (±100 volts). If the input signal is not known, begin with X100 attenuation and decrease as required.

The SLOPE switch selects whether the instrument triggers on the positive or negative going edge of the input waveform. For sinusoidal waveforms, the choice is usually arbitrary, but for other waveforms it is desirable to trigger on the steepest slope in order to minimize trigger error.

The TRIGGER LEVEL control sets the triggering point on the input waveform at any level between +1 and −1 volt. For input signals that cross ground level, the trigger level can be preset at zero crossover.

For the correct input circuit adjustment proceed as follows:

a) Set the FUNCTION switch to COUNT START
b) Connect a signal to the Channel A BNC connector
c) Set the Coupling and SLOPE switches as explained above
d) Set ATTENUATOR switch to X100 and rotate the Channel A TRIGGER LEVEL control from fully counter-clockwise to fully clockwise observing the points at which the counting stops. Decrease attenuation until proper counting is obtained through an angle of rotation of 45 degrees approximately.
e) Set the TRIGGER LEVEL control about midway between the 45 degree angle as outlined above.

During adjustment, the point of the waveform at which the counter is triggered may be observed on a high-input impedance oscilloscope connected to the A out pin on the rear panel.

The B Channel should be adjusted in the same way but in place of the display, an oscilloscope connected to B out on the rear should be used for the correct count observation.

NOTE

To minimize interchannel crosstalk due to high amplitude input signals in the TIME A→B and A/NB Modes of operation low impedance termination (50 ohms) should be connected to the BNC input connectors. Otherwise the input signals should be attenuated before its application to the counter's inputs.

3-5. PERFORMANCE TEST

The 5500A has a built-in test circuit that provides a confidence check of the instrument's operation. This circuit is used in the CHK Mode, which checks most of the circuitry in the instrument.

The performance of the 5500A should be checked upon receipt from the factory, after maintenance has been performed, and before each use.

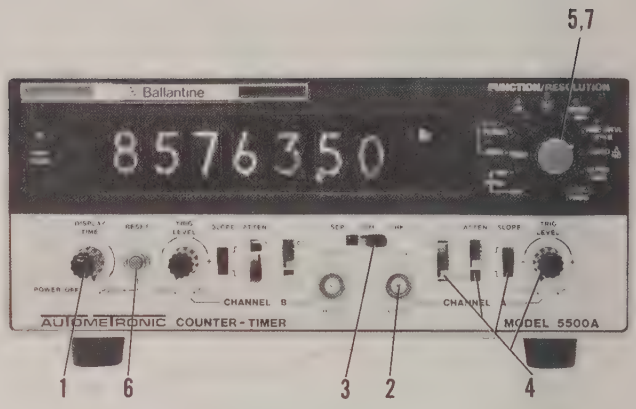
1. Set the SEP-COM-CHK switch to the CHK position
2. Adjust both input circuits as outlined in paragraph 3-4
3. Set the FUNCTION switch to COUNT STOP
4. Press the RESET push-button and check that all digits display "0"
5. Set FUNCTION switch to COUNT START and check that the counter totalizes, overflows and the GATE light is on with the RESOLUTION switch set to 4,5,6 or 7 digits resolution
6. Set FUNCTION switch to COUNT STOP. Check that the GATE light goes out and the display is held
7. Set FUNCTION switch to FREQ. The display should read:
   1.000 MHz with 4 digit resolution ±1 count
   1000.0 KHz with 5 digit resolution ±1 count
   1000.00 KHz with 6 digit resolution ±1 count
   1000.000 KHz with 7 digit resolution ±1 count
8. Set FUNCTION switch to PERIOD. The display should read 1.0 μsec ±1 count
9. Set FUNCTION switch to positive pulse mode. The display should read 0.5 μsec ±1 count. Note: slight readjustment of the Channel A TRIG LEVEL control may be necessary to obtain this reading
10. Set FUNCTION switch to negative pulse mode. The display should read 0.5 μsec ±1 count. Note: slight readjustment of the Channel A TRIG LEVEL control may be necessary to obtain this reading
11. Set FUNCTION switch to PERIOD AVG. The display should read 1.000 μsec ±1 count
12. Set FUNCTION switch to TIME A→B. The display should read 1.0 μsec ±1 count with both switches set to positive or negative slopes, and 0.5 μsec ±1 count when the SLOPE switches are set to opposite polarity. Note: slight readjustment of Channel A TRIGGER LEVEL control may be necessary to obtain the readings
13. Set FUNCTION switch to A/NB. The display should read 1.000 ±1 count
14. Set FUNCTION switch to TIME INTVL. Short pin 23 of the REMOTE PROG connector to ground (if option 11 is installed in this instrument) or short the two binding posts (with option 11 not installed). Observe for correct timing on the display

3-6. OPERATING PROCEDURES

Paragraphs 3-7 through 3-14 describe typical operating procedures.

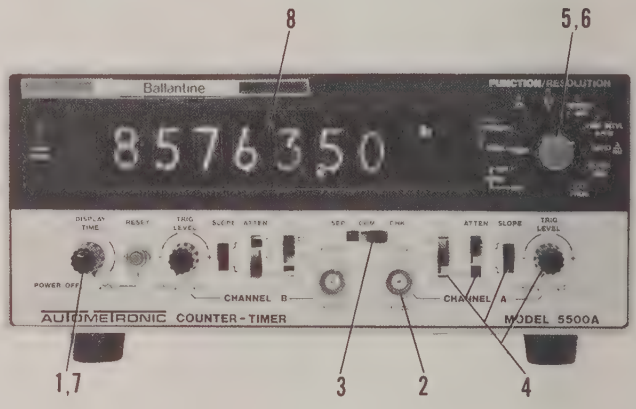
3-7. Operation in COUNT mode

1. Turn power switch on
2. Connect signal to be counted to the Channel A connector
3. Set SEP-COM-CHK switch to SEP
4. Adjust the Channel A input circuit as outlined in paragraph 3-4.
5. Set FUNCTION switch to COUNT STOP
6. Press RESET pushbutton
7. Start counting by setting the FUNCTION switch to COUNT START and stop by setting to COUNT STOP. Note: If the OVERRANGE indicator is lit, the count indicated is not the total count



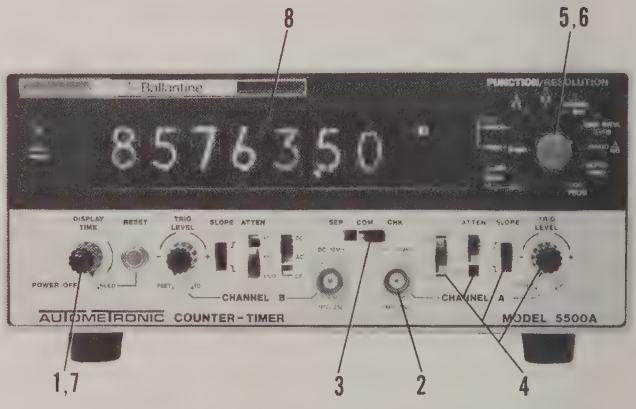
3-8. Operation in FREQ mode

1. Turn power switch on
2. Connect signal to be measured 0 to 70 MHz to the Channel A connector
3. Set SEP-COM-CHK switch to SEP
4. Adjust the Channel A input circuit as outlined in paragraph 3-4
5. Set FUNCTION switch to FREQ
6. Set RESOLUTION switch to required resolution
7. Adjust DISPLAY TIME control for convenient measurement interval
8. The display indicates the frequency of the input signal. The unit and decimal point is internally computed and displayed automatically.



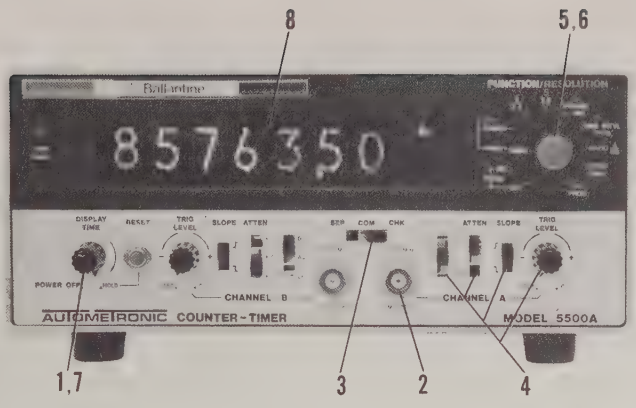
3-9. Operation in PERIOD mode

1. Turn power switch on
2. Connect signal to be measured (100 nsec to 10^7 seconds) to the Channel A connector
3. Set SEP-COM-CHK switch to SEP
4. Adjust the Channel A input circuit as outlined in paragraph 3-4
5. Set FUNCTION switch to PERIOD
6. Set the RESOLUTION switch to the required resolution
7. Adjust DISPLAY TIME control for convenient measurement interval
8. The display indicates the period of the input signal. The unit and decimal point is internally computed and displayed automatically



3-10. Operation in Positive Pulsewidth and Negative Pulsewidth modes

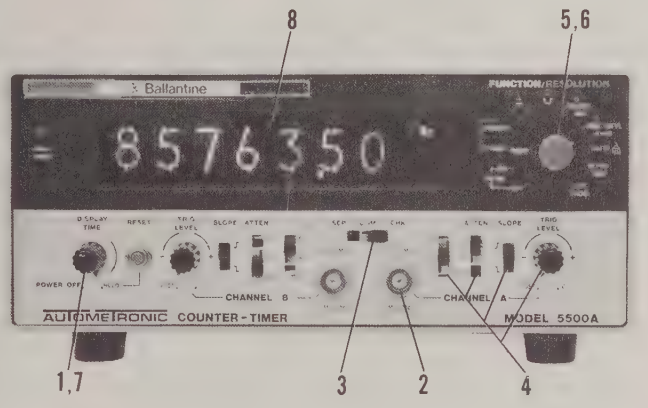
1. Turn power switch on
2. Connect signal to be measured (100 nsec to 10^7 seconds) to the Channel A connector
3. Set SEP-COM-CHK switch to SEP
4. Adjust the Channel A input circuit as outlined in paragraph 3-4
5. Set FUNCTION switch to positive pulsewidth or negative pulsewidth
6. Set RESOLUTION switch to the required resolution
7. Adjust DISPLAY TIME control for convenient measurement interval
8. The display indicates the width of the positive or negative pulse. The unit and decimal point is internally computed and displayed automatically



3-11. Operation in the PERIOD AVG mode

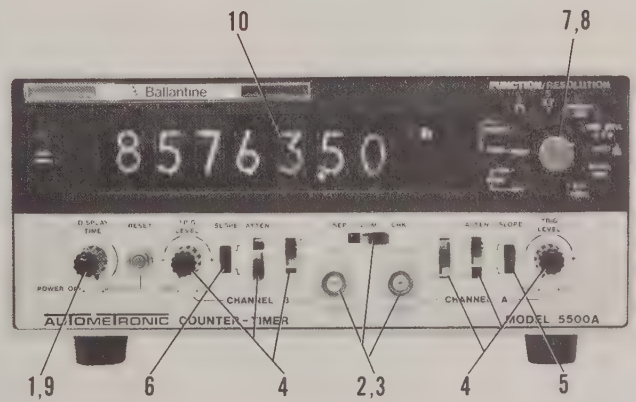
1. Turn power switch on
2. Connect signal to be measured (0.1 Hz to 1 MHz) to the Channel A connector
3. Set SEP-COM-CHK switch to SEP
4. Adjust the Channel A input circuit as outlined in paragraph 3-4
5. Set FUNCTION switch to PERIOD AVG
6. Set RESOLUTION switch to the required resolution
7. Adjust DISPLAY TIME control for convenient measurement interval
8. The display indicates the average period of the input signal in microseconds

   Note: In this mode, the display range may be exceeded if the minimum frequency of the input signal is less than:
   100 Hz with 4 digit resolution
   10 Hz with 5 digit resolution
   1 Hz with 6 digit resolution
   0.1 Hz with 7 digit resolution



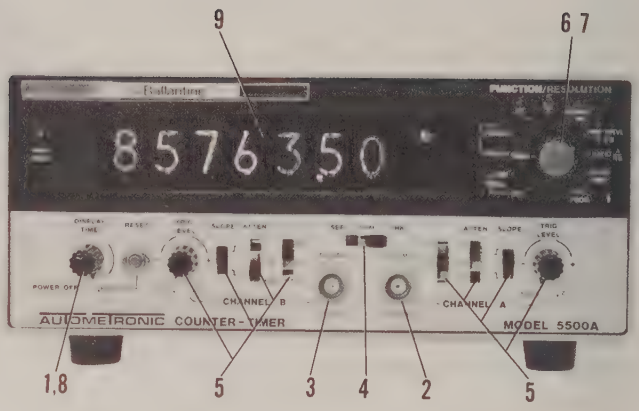
3-12. Operation in Time A→B mode

1. Turn power switch on
2. If separate start and stop signals are to be used, set SEP-COM-CHK switch to SEP. Connect the start signal to Channel A connector and connect the stop signal to Channel B connector
3. If one signal is to be used to start and stop the count, set SEP-COM-CHK switch to COM. Connect the signal to Channel A connector
4. Adjust the Channel A and Channel B input circuits as outlined in paragraph 3-4
5. Set the Channel A SLOPE switch to start the count on the desired slope
6. Set the Channel B SLOPE switch to stop the count on the desired slope
7. Set FUNCTION switch to TIME A→B
8. Set RESOLUTION switch to required resolution
9. Adjust DISPLAY TIME control for convenient measurement interval
10. The display indicates the time interval between the start signal at Channel A and stop signal at Channel B. The unit and decimal point is internally computed and displayed automatically



3-13. Operation in Ratio (A/NB) mode

1. Turn power switch on
2. Connect higher frequency input (0 to 70 MHz) to Channel A connector
3. Connect lower frequency input (0 to 10 MHz) to Channel B connector
4. Set SEP-COM-CHK switch to SEP
5. Adjust the Channel A and Channel B input circuits as outlined in paragraph 3-4
6. Set FUNCTION switch to A/NB
7. Set RESOLUTION switch to required resolution
8. Adjust DISPLAY TIME control for convenient measurement interval
9. The display indicates the ratio FA/FB with an automatically positioned decimal point



3-14. Operation in TIME INTVL mode

1. Turn power switch on
2. Set FUNCTION switch to TIME INTVL
3. Set RESOLUTION switch to required resolution
4. Press the RESET push-button
5. Short pin 23 of REMOTE PROG connector to ground, pin 24, (if option 11 is installed in this instrument) or short the two binding posts (option 11 not installed) to start the timing interval, and open the terminals to stop the timing interval. This action may be repeated as many times as required
6. The display indicates the total time of operation. The unit and the decimal point is internally computed and displayed automatically

Principles of Operation

4-1. INTRODUCTION

This section of the manual contains a description of the circuitry used in the 5500A. A simplified block diagram is given in Figure 4-1 followed by signal Flow-Diagrams for each mode of operation (Fig. 4-2 to Fig 4-9). Complete schematics of each circuit are given in Section 7. Refer to these diagrams throughout the following circuit description.

4-2. ASSEMBLY DESIGNATIONS

Table 4-1 lists the designations of the assemblies used in this instrument.

Table 4-1. Assembly Identification

ASSY	NAME
A1	Front Panel Assy
A2	Rear Panel Assy
A3	Main P.C. Board Assy
A4	Display P.C. Board Assy
A5	Input Circuits Assy
A6	Chassis Assy
A7	Interconnect

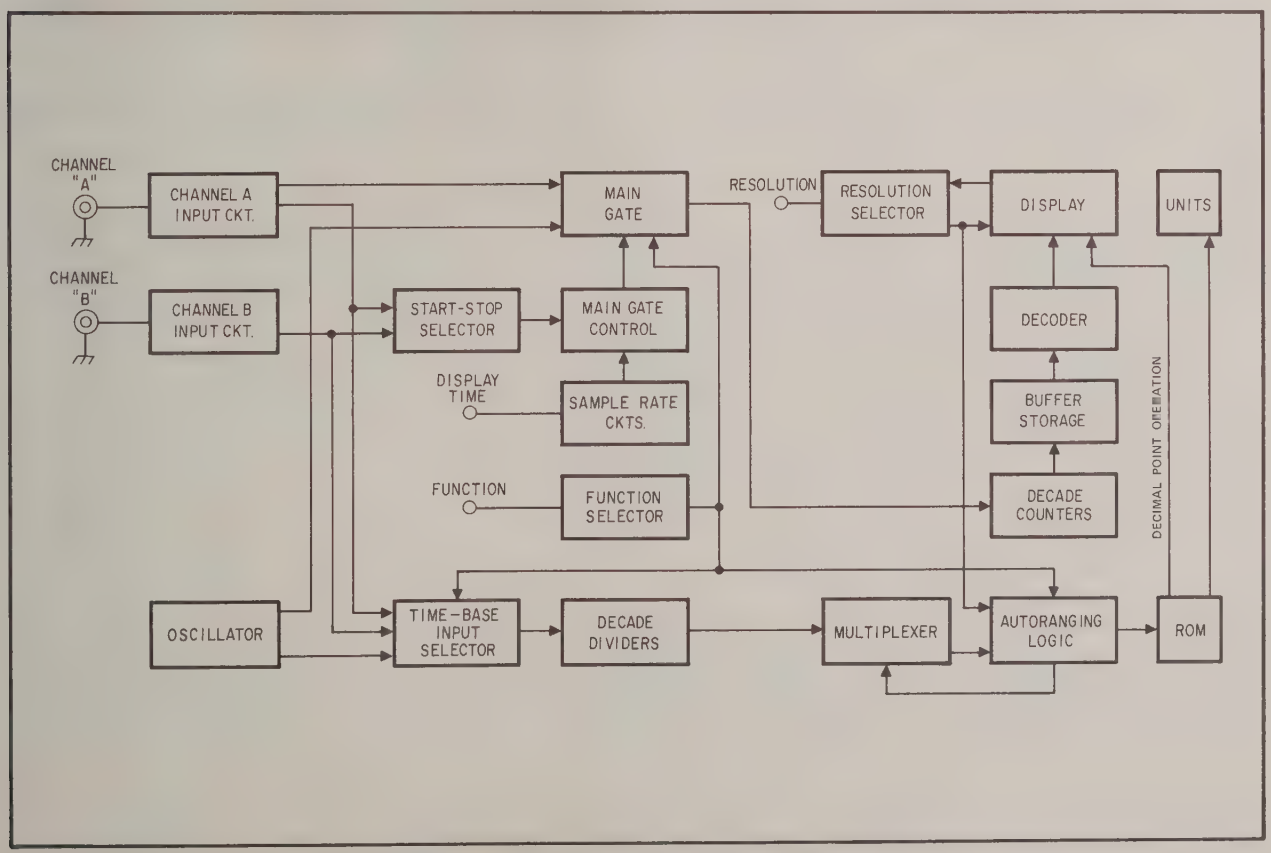


Figure 4-1. 5500A Simplified Block Diagram

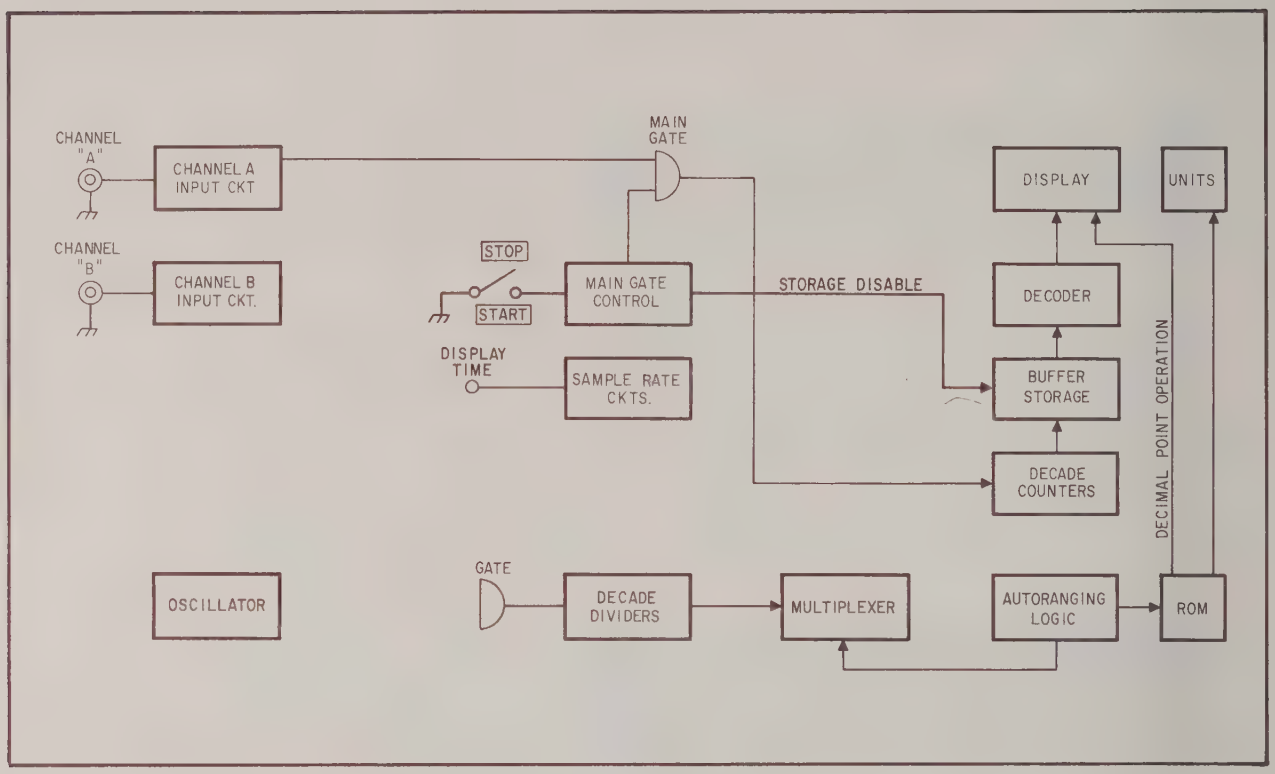


Figure 4-2. Count Mode Flow Diagram

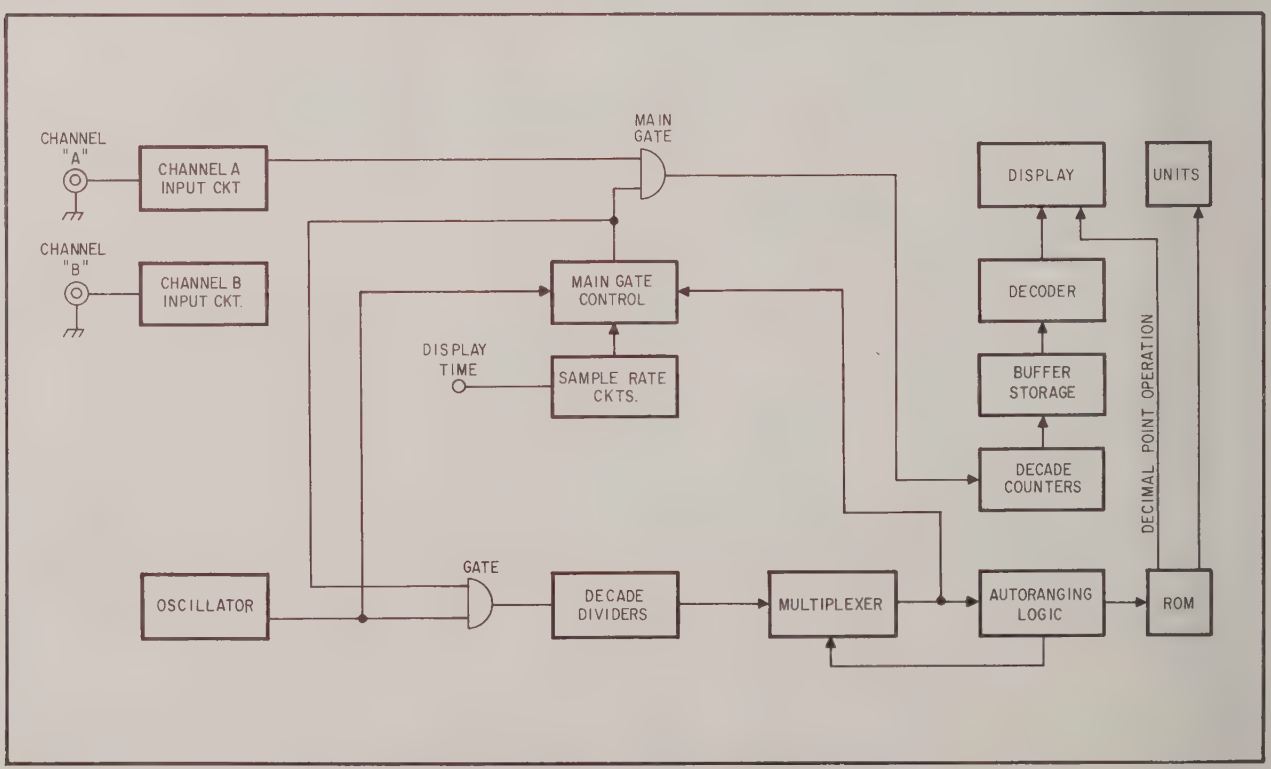


Figure 4-3. Frequency Mode Flow Diagram

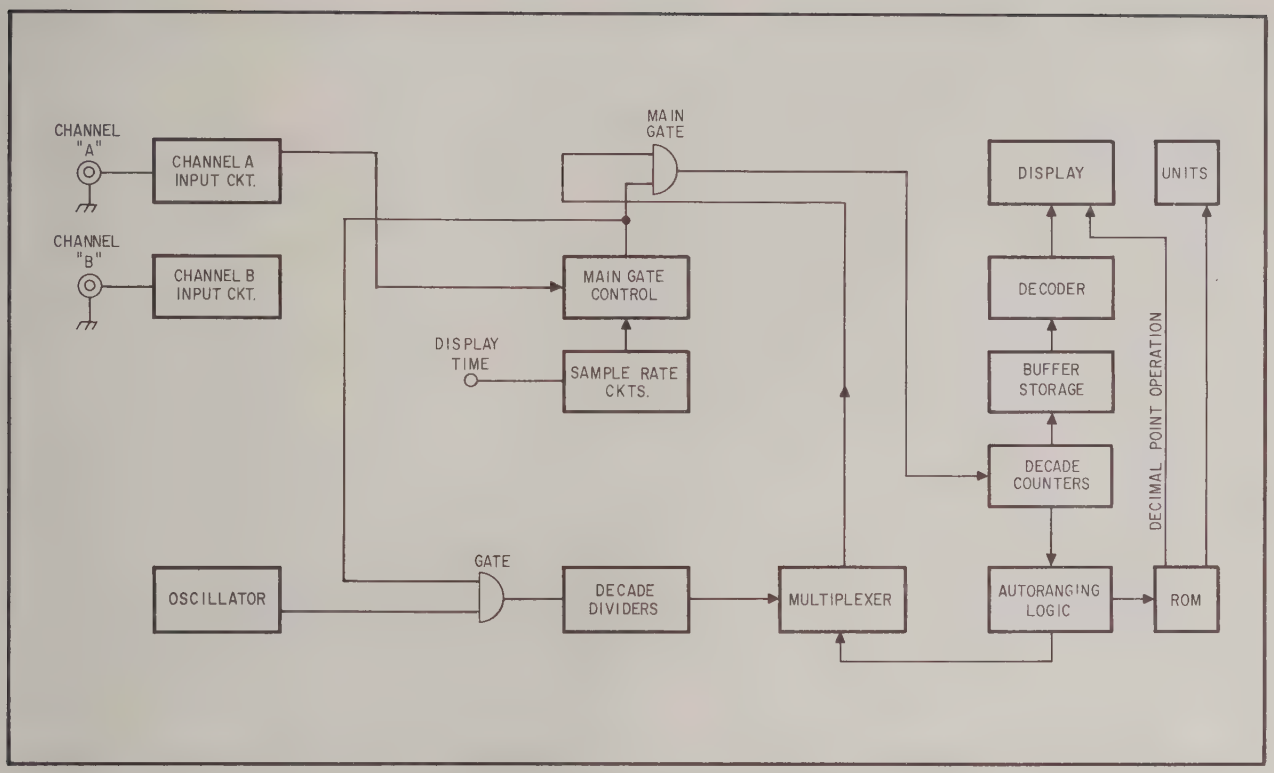


Figure 4-4. Period Mode Flow Diagram

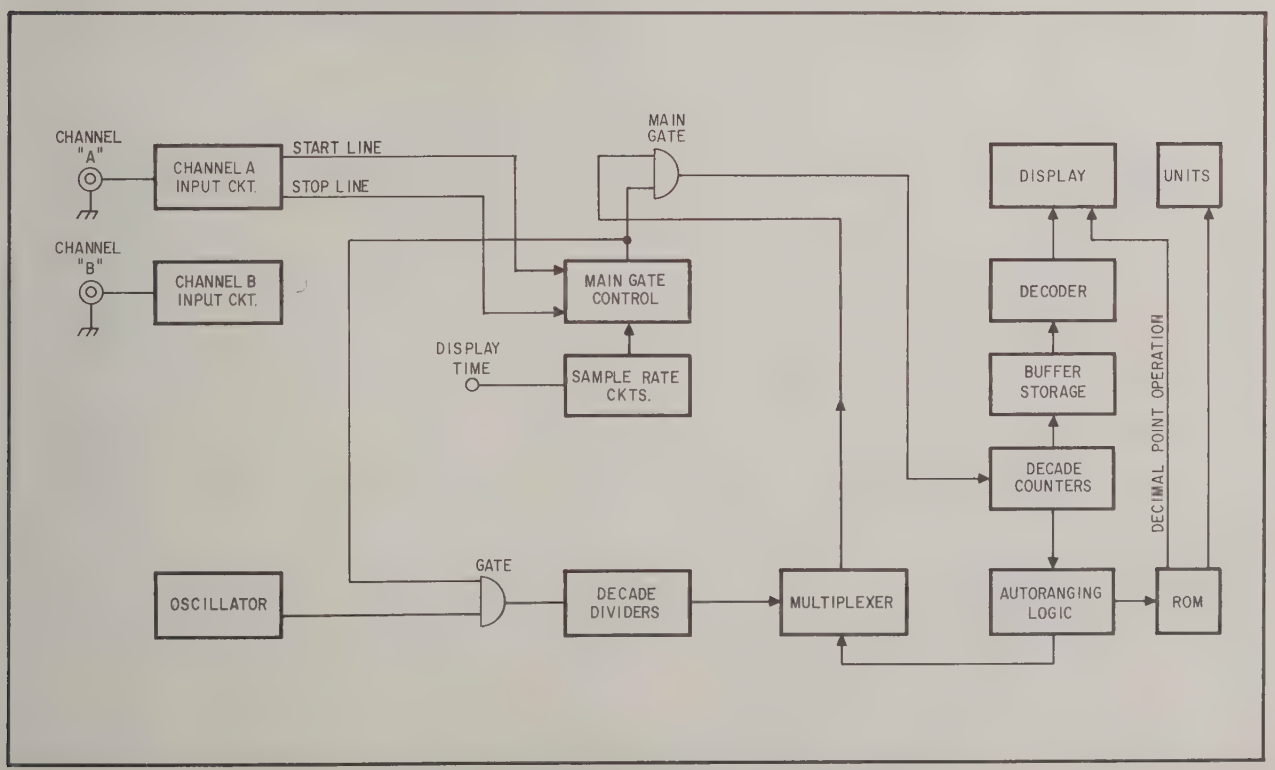


Figure 4-5. Positive or Negative Pulsewidth

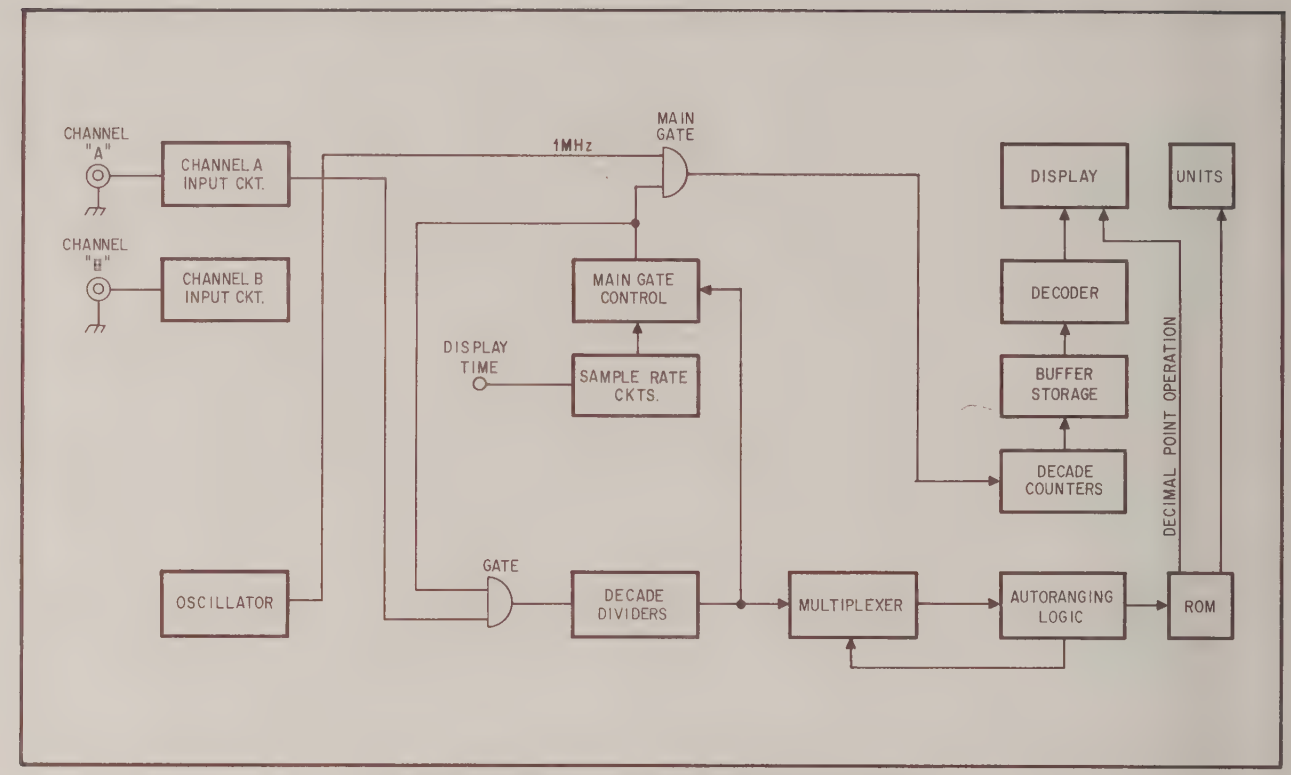


Figure 4-6. Period Average Mode Flow Diagram

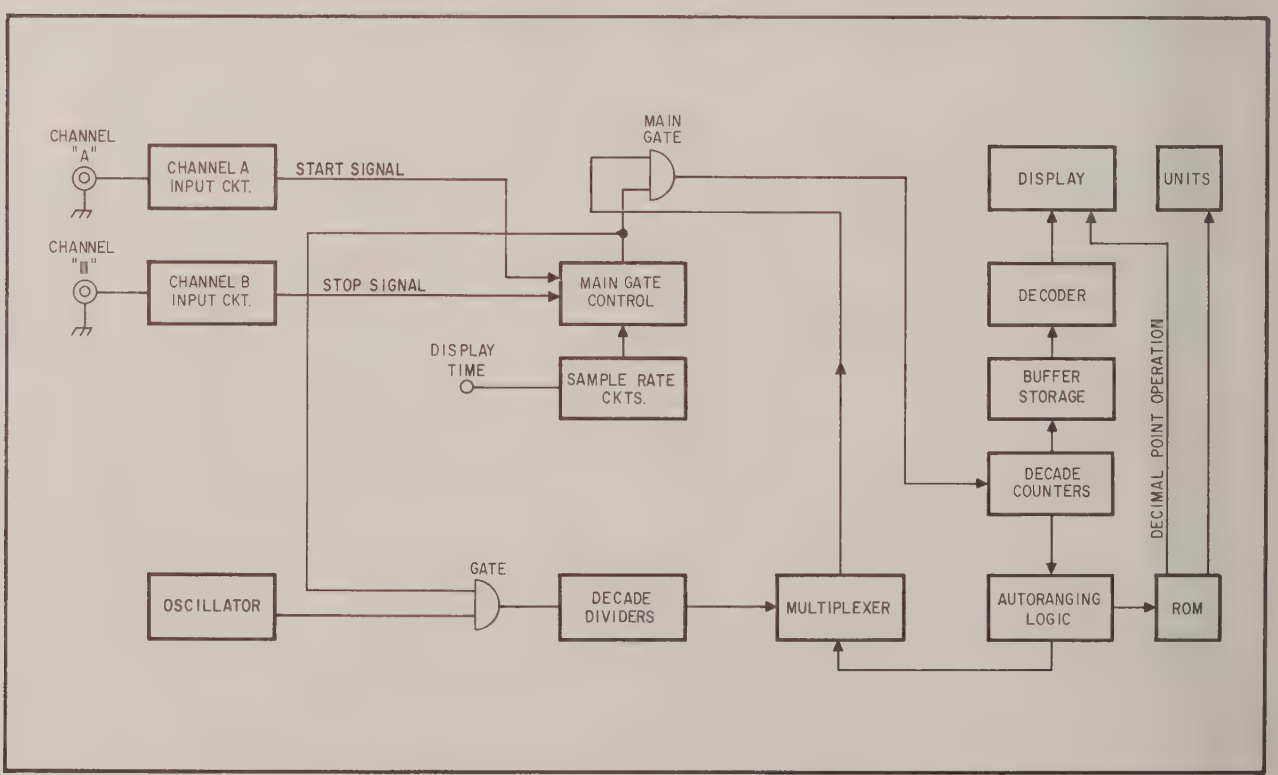


Figure 4-7. Time A→B Mode Flow Diagram

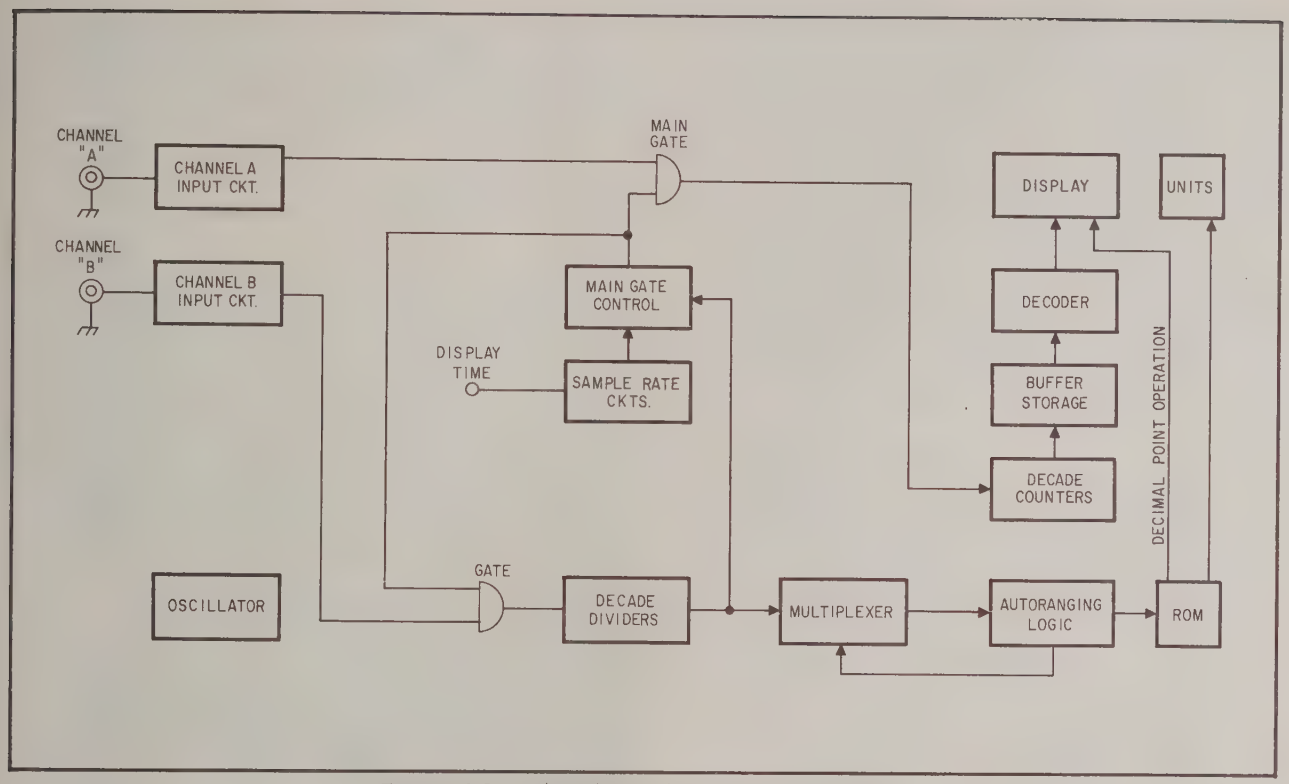


Figure 4-8. A/NB (Ratio) Mode Flow Diagram

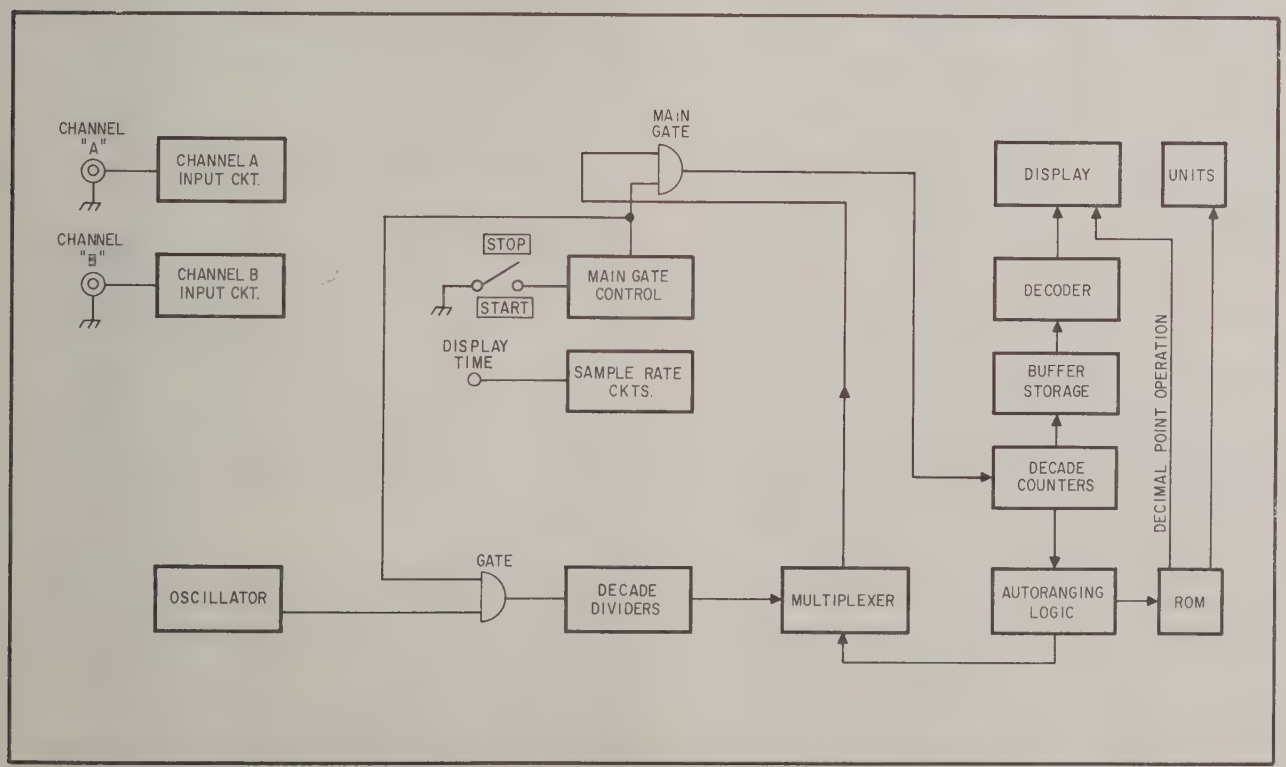


Figure 4-9. Time Interval Mode Flow Diagram

4-3. CHANNEL A INPUT CIRCUIT OPERATION

The 5500A has two input circuits, which are designated A and B. The Channel A input is used for all signal measurements. The B input is an auxiliary input and is used when measuring Time A→B and the ratio of two frequencies. Both circuits shape the input signal to provide well defined edges for proper triggering.

The Channel A input signals are routed through A1J1 to Coupling Selector A1S6. Depending on the switch setting, the signals are either directly coupled to Attenuator A1S5 (DC position) or taken via capacitor A1C1 (AC position). In the HF REJ position, capacitor A1C5 is connected to ground and causes signals above 1 kHz to be attenuated.

When Attenuator A1S5 is set to X1, the full input signal is fed via SEP-COM-CHK switch A1S13 to the gate of A5Q1A. With A1S5 set to X10 or X100, the appropriate voltage divider is selected. The SEP-COM-CHK switch connects inputs A and B in parallel when set to COM, and connects a 1 MHz test signal to the A and B input circuits when set to CHK.

The signal to A5Q1A and A5Q1B is limited by the diode-limiter A5CR1 and A5CR2. The limiter protects FET A5Q1A from overload. TRIG LEVEL control A1R9 selects the gate voltage of A5Q1B between −1 V and +1 V approx. and thereby determines the triggering level. Maximum sensitivity is obtained when the triggering voltage is about zero volts. This obtained when the TRIG LEVEL control is set to its mid position. A5R6 is a balance potentiometer which compensates for tolerances in the differential amplifier circuit.

The outputs of A5Q1A A5Q1B drive the emitter followers A5Q2 A5Q3. This, in turn, drives differential amplifier A5Q4 A5Q5, the output of which is taken to the current amplifier A5Q6 A5Q7. The output of A5Q7 is coupled through emitter follower A5Q8 to the input of Schmitt trigger A5Q9 A5Q10. The Schmitt trigger shapes the input waveform to provide well defined edges for proper triggering.

4-4. CHANNEL B INPUT CIRCUIT OPERATION

The Channel B input signals are routed through A1J2, Coupling Selector A1S7 and Attenuator A1S8 to the gate of A5Q12A. The Coupling Selector and Attenuator are identical to those in the Channel A input circuit. Transistors A5Q12A, A5Q12B, A5Q13 and A5Q14 with their associated circuitry form a differential amplifier whose output is fed to the input of the integrated circuit Schmitt Trigger (U4) which shapes the waveforms of the Channel B signal.

4-5. 10 MHz OSCILLATOR OPERATION

The 10 MHz oscillator consists of transistors A3Q1 and A3Q2 acting as a buffer. A3Q1 operates as an amplifier with positive feedback. It forms a very stable crystal-controlled oscillator, which can be adjusted to exactly 10 MHz by means of trimmer capacitor A3C1. The oscillator output is fed to Nand gate A3U10D through buffer amplifier A3Q2, which minimizes the loading of the oscillator and prevents frequency variations due to loading.

4-6. EXT CLOCK IN / 1 MHz CLOCK OUT OPERATION

Connector A2J1 is used as an input point for an external clock and also for the output of a 1 MHz signal from the instrument. With switch A2S1 set to 1 MHz CLOCK OUT, Nand gate U10D is enabled and the 10 MHz internal clock is fed to decade divider U1. The 1 MHz clock signal at the output of U1 is supplied to the circuitry of the instrument and to A2J1. When the switch is set to EXT CLOCK IN, Nand gate U10B is enabled and the output of the Schmitt trigger A3U9 is routed to the decade divider A3U1. When externally triggered, the input to A3U9 is protected against overload by a pair of diodes A3CR1 A3CR2.

4-7. CONTROL LOGIC OPERATION

The control logic determines the start and stop functions for the count being taken, controls the routing of input and time base signals, and the sequence of operation. The operation of the control logic will be described by an analysis of three of the operating modes.

Consider the operation of the circuitry in the COUNT mode. With FUNCTION switch A1S1 set to COUNT START, the inputs to Nand gates A3U14C and A3U14D are low. The outputs of both gates are therefore high. This level is inverted to a low at pin 6 of A3U14B. The high gate signal output from A3U14A enables main gate A5U1C contained on the input circuit board. Counting will continue until the FUNCTION switch is set at COUNT STOP.

With the FUNCTION switch set at FREQ position, ground is applied to Nand gate A3U19A and inverter A3U18C. The high at the output of A3U19A enables A3U16A and A3U2A, and the high at the output of A3U18C enables A3U8B. All the inputs to Nand gate A3U20B are high and the low at the output of the gate inhibits A3U16D. Main gate control flip-flops A3U15A and A3U15B are initially reset and the low at the Q output of A3U15B inhibits Nand gate A3U4C and enables Nand gates A3U4A and A3U8B. 1 MHz clock pulses are therefore routed through A3U8B, A3U8E, A3U16A, A3U16E, A3U4A and A3U4B to the clock input of D flip-flop A3U15B.

The first positive-going edge of the 1 MHz clock caused the Q output of A3U15B to adapt the state of the D input (i.e. logic high). In this state, all the inputs to A3U4C are high and the low at the output of the gate prevents subsequent 1 MHz clock pulses from reaching the clock input of A3U15B. The low at the Q output of A3U15B toggles A3U15A to the set state and makes the gate signal at the output of A3U14A go high.

While the gate signal is high, the output of the Channel A input circuit is routed to the first decade counter stage. Nand gate A3U13B is also enabled, allowing the 1 MHz clock pulses to be routed to the time base multiplexer. This circuit, together with the autoranging logic comprising Nand gates A3U2A, A3U2D and decade counter A3U12, produces a succession of pulses at decade intervals. These pulses are counted by the decade counter.

When the first four digits of the display have been filled (with RESOLUTION switch set to 5), or more exactly, when a count of 9900 is reached, the trigger input to J-K flip-flop A3U5A goes low and sets the flip-flop. When A3U5B is reset by the next pulse from the time base multiplexer, both inputs to Nand gate A3U17B are high and the low at its output sets flip-flop A3U4A, A3U4B. The low at the output of A3U4B is inverted to a high by A3U4C, which enables A3U4A. The next 1 MHz clock pulse is therefore routed to the clock input of A3U15B. Since its D input is low (because A3U15A is set) the positive going edge of the 1 MHz clock makes the Q output of A3U15B go low, thereby ending the count interval.

The autoranging circuit, together with the circuit in the display unit which detects when a count of 9900 is reached, automatically selects the optimum gate time for maximum resolution, whilst preventing the display capacity from being exceeded. The time base multiplexer provides all the necessary timing signals beginning with a start pulse to initiate the measurement. This is followed by a succession of valid stop pulse at decade intervals of 1 μsec, 10 μsec, 100 μsec and so on up to 1 sec. The first available stop pulse following the 9900 count is detected by J-K flip-flops A3U5A and A3U5B. The number of stop pulses counted by decade counter A3U12 before the display was filled determines the decimal point and unit information.

Operation is PERIOD mode is similar to operation in FREQ mode. However, in PERIOD mode the instrument counts the internal clock during one period of the input signal. Also, the decade counter in the autoranging circuit counts the "overflow" pulses from the most significant decade of the display unit, instead of the stop pulses from the time base multiplexer.

With the FUNCTION switch set at PERIOD, ground is applied to Nand gates A3U4C and A3U20B. The high at the output of A3U4C enables A3U4A, and the high at the output of A3U20B enables A3U16D, A3U17A and A3U8C. The low at the output of inverter A3U18B inhibits A5U1A in the input circuits board. The signal from the Channel A input circuit is routed through A5U1D, the Channel A slope selection circuit A3U16D, A3U16E, A3U4A and A3U4B to the clock input of D flip-flop A3U15B. The first positive going edge of the Channel A signal causes the Q output of A3U15B to go high. The low at the $\overline{Q}$ output sets A3U15A and makes the gate signal at the output of A3U14A to high.

The Channel A slope selection circuit comprises SLOPE switch A1S4, and gates A3U31A to A3U31D and N or gates A3U31E, F. The circuit determines whether counting occurs between positive or negative edges of the input signal. When the switch is set at positive slope, ground is applied to Nand gate A3U31D and therefore the negative going pulses from the input circuit are routed to the main gate control circuit.

When the gate signal goes high, 10 MHz clock pulses are routed through A3U8C, A3U8E and A3U13B to the time base multiplexer. The output is fed through A3U17A and A3U17C to the base of A5Q15 on the input circuit board. Since A5U1C is also enabled, the internal clock is fed to the first decade counter stage. When the second positive-going edge of the Channel A signal appears, A3U15B changes state, thereby ending the count interval. The cycle is repeated when a reset pulse is generated.

While the instrument is counting, overflow pulses from the most significant decade are routed through A3U2C and A3U2D to decade counter A3U12. Until an "overflow" occurs, pulses at the highest time base frequency (0.1 μsec) are routed to the first counter stage. When an overflow occurs, the next lower time base frequency is selected (1 μsec). This process continues until the end of the count interval. The output of decade counter A3U12 provides the correct decimal point and unit indication.

4-8. SAMPLE RATE AND RESET CIRCUIT

In order to ensure sufficient time for a visual readout of the measurement, a Display Time control is provided at the front panel of the instrument. The purpose of this control is to provide a reset pulse for a selected time interval (0.2 to 5 seconds) after completion of a measurement. When the control is set to HOLD, the display is held indefinitely until the manual RESET pushbutton is depressed.

During the count interval, transistor A3Q1 is in saturation due to the high on its base from the main gate control circuit. At the end of the count interval, A3Q7 is cut-off and causes capacitor A3C17 to start to charge. When the voltage across the capacitor reaches the unijunction transistor A3Q8 firing voltage, a negative-going pulse is produced and supplied to the Reset Multivibrator, U30B and Q10. The output from A3Q10 resets the circuits in the instrument. A reset pulse can also be produced manually by operation of the RESET pushbutton A1S11. Setting of the DISPLAY TIME control to HOLD will cause the +15 V supply to be disconnected from the DISPLAY TIME control. Under this condition, A3C17 will not be charged and therefore no reset pulse will be generated.

The inhibit input is normally intended for use with an external digital printer, but if necessary it can also be used independently to provide an external form of display control. A high level at A2J2-22 will saturate A3Q8 and thereby inhibit the generation of a reset pulse.

4-9. GATE INDICATOR, TRANSFER PRINT COMMAND CIRCUITS

The gate indicator circuit controls the lighting of the GATE lamp. The output of Nand gate A3U14A, which is high during the count interval, is supplied through inverter A3U6C to Nand gate A3U28A and the pulse stretcher comprising A3U28B and A3U28D. The output of A3U28A is supplied to the display circuit for controlling the lighting of the GATE indicator. For short count intervals the pulse stretches causes the GATE lamp to light for a longer interval, enabling it to be visible even when the count interval is very short.

The transfer circuit generates a positive-going pulse which transfers the content of the counting circuits to the storage and display units. The circuit also controls the transfer of decimal point and units information. The transfer pulse is generated automatically at the end of the count interval.

The print command circuit produces a positive-going pulse that instructs a digital printer to record the BCD information from the display circuits. The circuit comprises monostable U30A, U32D and transistor A3Q5.

4-10. DISPLAY CIRCUIT

The display circuit consists of seven decimal/BCD counter latch circuits and BCD/decimal decoders which drive numeric display tubes. The display circuit contains also a coincidence circuit, a resolution selection circuit and circuits for lighting the decimal points in the display tubes and for lighting the GATE, OVERRANGE and units indicators.

The 10^{0} decimal counter comprises Shottky flip-flops U2 U3, which are contained on the input circuits board. It counts the signal on the count line and when it reaches a count of 10, it produces a carry pulse which is counted by the 10^{1} decimal/BCD counter. The 10^{1} counter drives the 10^{2} counter, etc., in a similar manner.

The BCD output of the counters is stored by the latch circuits. With a logic "0" at the transfer terminals, the previous count is displayed. When a logic "1" appears, the count is transfered to the decoders.

Nand gate U2 is used to detect when a count of 999900 is reached. When this occurs, all the inputs to the gate are high and therefore the output goes low. This level causes the autoranging logic to select the first available stop pulse and thus end the gate time.

The number of stop pulses counted by the autoranging logic determines the decimal point and units display.

RESOLUTION switch A1S2 serves several functions. Its main function is to select the number of display digits required. +200 is routed through the slider of wafer A to the anode of DS5 in position 5, to the anode of DS6 in position 6, and to the anode of DS7 in position 7. The anodes of DS1 to DS4 are connected permanently to +200 V.

The RESOLUTION switch is also used to route an overflow pulse from the most significant decade to the autoranging logic (timing modes) and to flip-flop U1C U1D (all modes). The logic level applied to the slider of wafer B is controlled by transistor A3Q6 and FUNCTION switch A1S1.

4-11. POWER SUPPLY

The power supply provides +200 V, ±15 V and +5 V. The instrument may be operated from a 115 volt or 230 volt ac source. Switch A2S3 provides the proper power transformer connection according to the source used.

The +200 V output is unregulated and is the supply voltage for the display tubes.

The +15 V output is regulated and is one of the supply voltages for the input circuit. A3Q17 is a series power transistor and A3U33 provides a constant reference voltage.

The +5 V output is the supply voltage for all of the micrologic. A6Q1 is the series regulator and is driven by the emitter follower A3Q14.

The −15 V output is regulated and is one of the supply voltages for the input circuit. A3Q11 and A3Q15 perform the same function as A3Q14 and A6Q1 in the +5 V supply. A3Q12 and A3Q13 form a differential amplifier to amplify the error voltage on the base of A3Q13.

Maintenance and Calibration

5-1. INTRODUCTION

This section provides maintenance, calibration and service information for the 5500A. Included are a table of recommended test equipment, input circuits adjustment, oscillator frequency adjustment and in-cabinet performance check which may be used to verify proper operation of the counter.

5-2. TEST EQUIPMENT

Recommended test equipment for troubleshooting, alignment and performance checking is listed in Table 5-1. Test instruments other than those listed may be used if their specifications equal or exceed the required characteristics.

5-3. INSTRUMENT COVER REMOVAL

To remove the top or bottom cover, unlock four quarter turn fasteners which secure cover to instrument. Then slide cover towards the top of instrument. To replace cover, reverse procedure.

WARNING

115/230 VAC and DC supply wires are exposed when either cover is removed. Disconnect the power cord while removing the covers.

5-4. CLEANING

The 5500A should be cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket and prevents efficient heat dissipation.

Thoroughly clean both the inside and outside of the instrument. Remove dust from inaccessible areas with low pressure compressed air or vacuum cleaner. Use alcohol applied with a cleaning brush to remove accumulations of dirt or grease from connector contacts and component terminals. Clean the exterior of the instrument and the front panel with a mild detergent mixed with water, applying the solution with a soft, lint-free cloth.

5-5. VISUAL INSPECTION

The 5500A should be inspected occasionally for such defects as broken connections, loose, broken or frayed wiring, dirty or pitted switch and connector contacts and cracked or broken printed circuit boards. Often, before a total or partial failure occurs, a deteriorating component can be located due to obvious discoloration, cracking or care must be taken if heat-damaged parts are located. Overheating is usually only a symptom of trouble. For this reason, it is essential to determine the actual cause of overheating before the heat-damaged part is replaced, otherwise, the damage may be repeated.

5-6. REPAIR AND REPLACEMENT

Repair and replacement of electrical and mechanical parts must be accomplished with due exercise of caution. Printed circuit component boards can become warped, cracked or burnt from excessive heat or mechanical stress. The following repair techniques are suggested to avoid inadvertant destruction or degradation of parts and assemblies.

Use ordinary 60/40 solder and a 35 to 40-watt pencil type soldering iron on the circuit board. The tip of the iron should be clean and properly tinned for best heat transfer to the solder joint. A higher wattage soldering iron may separate the circuit from the base material. To desolder components use a commerical "solder sipper".

Always replace a component with its exact duplicate as specified in the parts list.

5-7. CHANNEL A INPUT CIRCUIT ADJUSTMENT

a. Connect a 50 kHz sinewave signal, 40 mV p-p, to the Channel A input.
b. Connect an oscilloscope or rms meter to the anode of CR6 (be carefull not to shorten to ground).
c. Set TRIG LEVEL to the PSET position.
d. Adjust trimpot R10 to maximum amplitude.
e. Connect oscilloscope probe to pin 2 of U1.
f. Adjust trimpot R17 for maximum symmetry.

Table 5-1. Recommended Test Equipment

REQUIREMENT	INSTRUMENT OR EQUIVALENT
50 kHz to 100 MHz, 5 mV to 5 V constant amplitude sinewave generator	Tektronix Type 191 Signal Generator
10 Hz to 10 MHz sinewave generator	HP Model 651A
Oscilloscope having dc to 40 MHz minimum bandwidth	Ballantine 1040A
Oscilloscope 15 MHz	Ballantine 1066A
Pulse Generator, 10 HZ to 50 MHz	EH Model G 710
1 MHz Frequency Standard	HP Model 105A/B
True RMS Voltmeter	Ballantine 323
Optional – Calibrator	Ballantine 6125A

Table 5-2. Frequency Mode Performance Check

NO	RESOLUTION SWITCH	INPUT AMPLITUDE mV p-p	FREQUENCY	READING
1	4	250	70 MHz	70.00 MHz
2	5	250	70 MHz	70.000 MHz
3	6	250	70 MHz	70000.0 KHz
4	7	250	70 MHz	70000.00 KHz
5	4	250	10 MHz	10.00 MHz
6	5	250	10 MHz	10.000 MHz
7	6	250	10 MHz	10000.0 KHz
8	7	250	10 MHz	10000.00 KHz
9	4	60	1 MHz	1.000 MHz
10	5	60	1 MHz	1000.0 KHz
11	6	60	1 MHz	1000.00 KHz
12	7	60	1 MHz	1000.000 KHz
13	4	60	100 KHz	100.0 KHz
14	5	60	100 KHz	100.00 KHz
15	6	60	100 KHz	100.000 KHz
16	7	60	100 KHz	0100.000 KHz
17	4	60	10 KHz	10.00 KHz
18	5	60	10 KHz	10.000 KHz
19	6	60	10 KHz	010.000 KHz
20	7	60	10 KHz	0010.000 KHz
21	4	60	1 KHz	1.000 KHz
22	5	60	1 KHz	01.000 KHz
23	6	60	1 KHz	001.000 KHz
24	7	60	1 KHz	0001.000 KHz
25	4	60	100 Hz	0.100 KHz
26	5	60	100 Hz	00.100 KHz
27	6	60	100 Hz	000.100 KHz
28	7	60	100 Hz	0000.100 KHz
29	1 sec	60	100 Hz	0000.100 KHz

5-8. CHANNEL B INPUT CIRCUIT ADJUSTMENT

a. Connect a 1 MHz sinewave signal, 40 mV p-p, to the Channel B input.
b. Connect probe of oscilloscope to pin 7 of IC4.
c. Set TRIG LEVEL control to the PSET position.
d. Adjust trimpot R45 for maximum symmetry.

5-9. TROUBLESHOOTING BY SELF-CHECK

When malfunction is suspected, disconnect all equipment from counter and perform self-check procedure given in Section 3. If counter does not self-check properly, refer to Section 4, Principles of Operation, for information on the operation of the circuits. If the counter self-checks properly, check that all inputs to counter are within the limits of specifications. If malfunction still occurs, cause is internal to counter. Make performance checks (par. 5-10) to help determine the source of trouble.

5-10. IN-CABINET PERFORMANCE CHECK

The following performance verifies proper operation of all circuits in the 5500A and may be used:

a. As part of an incoming inspection check of instrument specifications.
b. Periodically, for instruments used in systems.
c. As part of troubleshooting procedure.
d. After any repairs or adjustments, before returning instrument to regular service.

5-10-1. Count Mode (Channel A)

1. Set TRIG LEVEL control to PSET.
2. Set SEP-COM-CHK switch to SEP.
3. Set DC-AC-HF REJ switch to DC.
4. Set ATTEN switch to X1.
5. Connect sinewave signal 5 Hz to 1 MHz, 0.5 V p-p approx to BNC input connector.
6. Press the RESET pushbutton.
7. Set FUNCTION switch to COUNT START.
8. Vary the frequency from 5 Hz to 1 MHz and verify correct counting for each digit separately.
9. Check the OVERRANGE indicator is operated when the counter capacity is exceeded for 4, 5, 6 or 7 digits resolution.
10. Set FUNCTION switch to COUNT STOP. Check that the count stops and the reading is hold.

5-10-2. Frequency Mode (Channel A)

1. Set FUNCTION switch to FREQ.
2. Set DC-AC-HF REJ switch to DC.
3. Set SEP-COM-CHK switch to SEP.
4. Set ATTEN switch to X1.
5. Adjust Input Circuit as per Section 3, par. 3-4.
6. Check the instrument according to Table 5-2. The exact input frequency is not important. Check for stable readings. The input BNC connector should be terminated into 50 ohms.

5-10-3. Period Mode (Channel A)

1. Set FUNCTION switch to PERIOD.
2. Set DC-AC-HF REJ switch to DC.
3. Set SEP-COM-CHK switch to SEP.
4. Set ATTEN switch to X1.
5. Adjust Input Circuit as per Section 3, par. 3-4, with a 100 nano-second pulse, 0.5 V amplitude and rate of 1 KHz approx. The input BNC connector should be terminated into 50 ohms.
6. Check the instrument according to Table 5-3. The exact input period is not important. Check for stable readings.

5-10-4. Positive and Negative Pulse Modes (Channel A)

1. Set FUNCTION switch to positive pulse.
2. Set DC-AC-HF REJ switch to DC.
3. Set SEP-COM-CHK switch to SEP.
4. Set ATTEN switch to X1.
5. Adjust input circuit as per Section 3 with a 20 μsec positive pulse and 1:4 duty ratio and 0.5 V amplitude.
6. Check for a reading of 20 μsec with the FUNCTION switch set to positive pulse and 80 μsec when set to negative pulse. Verify that the slope switches do not influence the readings.

5-10-5. Period Average Mode (Channel A)

1. Set FUNCTION switch to PERIOD AVG.
2. Set DC-AC-HF REJ switch to DC.
3. Set SEP-COM-CHK switch to SEP.
4. Set ATTEN switch to X1.
5. Set TRIG LEVEL control to PSET.
6. Connect sinewave signal 5 Hz to 1 MHz, 0.5 V p-p, to BNC input connector.
7. Check the instrument according to Table 5-4.
8. Check 10 Hz (100 msec) signal with 4 digit resolution. Verify that the OVERRANGE indicator lights up.

5-10-6. Time A→B Mode

1. Set FUNCTION switch to TIME A→B.
2. Set DC-AC-HF REJ switch to DC (Channel A).
3. Set SEP-COM-CHK switch to SEP.
4. Set ATTEN switch to X1.
5. Set the DISPLAY TIME control to about midway.
6. Set the SLOPE switches of Channels A and B according to Table 5-5. Verify the opening of the counter gate while rotating the Channel A TRIG LEVEL control from fully clockwise (+) to fully anticlockwise (−), or the opposite, and the closure of the gate, in the same way for Channel B.
7. Set SEP-COM-CHK switch to COM.
8. Adjust input circuit as per Section 3, par. 3-4, with a 20 μsec positive pulse and 1:4 duty ratio and 0.5 V amplitude.
9. Set SLOPE switches of Channels A and B according to Table 5-6 and verify the correct readings.

Table 5-3. Period Mode Performance Check

NO	RESOLUTION SWITCH	RATE	PERIOD	READING
1	4	0.1 Hz	10 sec	10.00 sec
2	5	0.1 Hz	10 sec	10.000 sec
3	6	0.1 Hz	10 sec	10000.0 msec
4	7	0.1 Hz	10 sec	10000.00 msec
5	4	1 Hz	1 sec	1.000 sec
6	5	1 Hz	1 sec	1000.0 msec
7	6	1 Hz	1 sec	1000.00 msec
8	7	1 Hz	1 sec	1000.000 msec
9	4	10 Hz	0.1 sec	100.0 msec
10	5	10 Hz	0.1 sec	100.00 msec
11	6	10 Hz	0.1 sec	100.000 msec
12	7	10 Hz	0.1 sec	100000.0 μsec
13	4	100 Hz	10 msec	10.00 msec
14	5	100 Hz	10 msec	10.000 msec
15	6	100 Hz	10 msec	10000.0 μsec
16	7	100 Hz	10 msec	010000.0 μsec
17	4	1 KHz	1 msec	1.000 msec
18	5	1 KHz	1 msec	1000.0 μsec
19	6	1 KHz	1 msec	01000.0 μsec
20	7	1 KHz	1 msec	001000.0 μsec
21	4	10 KHz	100 μsec	100.0 μsec
22	5	10 KHz	100 μsec	0100.0 μsec
23	6	10 KHz	100 μsec	00100.0 μsec
24	7	10 KHz	100 μsec	000100.0 μsec
25	4	100 KHz	10 μsec	010.0 μsec
26	5	100 KHz	10 μsec	0010.0 μsec
27	6	100 KHz	10 μsec	00010.0 μsec
28	7	100 KHz	10 μsec	000010.0 μsec
29	4	1 MHz	1 μsec	001.0 μsec
30	4	3.3 MHz	0.3 μsec	000.3 μsec

5-10-7. A/NB (Ratio) Mode

1. Set FUNCTION switch to A/NB.
2. Connect internal oscillator output from rear panel BNC (1 MHz) to Channel A input. Adjust input circuit as per par. 3-4.
3. Set SEP-COM-CHK switch to SEP.
4. Connect sinewave oscillator to Channel B input. Adjust input circuit as per par. 3-4. Terminate into 50 ohms.
5. Check the instrument according to Table 5-7. The exact input frequency of Channel B is not important. Check for stable readings.

5-10-8. Time-Interval Mode

1. Set FUNCTION switch to TIME INTVL.
2. Shorten the REMOTE PROG jacks on the rear panel to start timing, and open to stop. For instruments equiped with Option 11 (Remote Programming), short pins 23 and 24 to start timing, and open to stop.
3. Observe correct timing and operation of the GATE indicator.

5-11. OSCILLATOR CALIBRATION

1. Trigger the oscilloscope from 1 MHz (Table 5-1) Frequency standard.
2. Observe 1 MHz signal from 1 MHz CLOCK OUT BNC on the rear panel of the 5500A on the vertical axis of the scope.
3. Adjust OSC ADJ trimmer on the rear panel of the 5500A with a plastic screwdriver until pattern on the oscilloscope stops drifting. It is important that this adjustment is made after at least 24 hours of continuous operation of the 5500A.

NOTE

NBS WWV standard ratio transmissions may also be used with a phase comparator system. Monitoring with a chart recorder is a good technique.

Instead of scope timebase triggering an X-Y lissajous figure is also recommended to observe proper 5500A clock frequency adjust.

Table 5-4. Period Average Performance Check

NO	RESOLUTION SWITCH	RATE	PERIOD	READING
1	4	1 MHz	1 μsec	1.000 μsec
2	4	100 KHz	10 μsec	10.00 μsec
3	4	10 KHz	100 μsec	100.0 μsec
4	4	1 KHz	1 msec	1000 μsec
5	5	100 Hz	10 msec	10000 μsec
6	6	10 Hz	100 msec	100000 μsec
7	7	5 Hz	0.2 sec	0200000 μsec

Table 5-5. Time A→B Performance Check

SLOPE A	SLOPE B	A TRIG LEVEL From → to	B TRIG LEVEL From → to
Pos Slope	Pos Slope	+ → −	+ → −
Pos Slope	Neg Slope	+ → −	− → +
Neg Slope	Neg Slope	− → +	− → +
Neg Slope	Pos Slope	− → +	+ → −

Table 5-6. Time A→B, Slope Selection Check

SLOPE A	SLOPE B	READING
Pos Slope	Pos Slope	100.0 μsec
Pos Slope	Neg Slope	020.0 μsec
Neg Slope	Neg Slope	100.0 μsec
Neg Slope	Pos Slope	080.0 μsec

Table 5-7. A/NB Ratio Mode

NO	RESOLUTION	CHANNEL B FREQUENCY	AMPLITUDE mV p-p	READING
1	4	10 MHz	130	0.100
2	4	1 MHz	60	1.000
3	4	100 KHz	60	10.00
4	4	10 KHz	60	100.0
5	4	1 KHz	60	1000
6	5	100 Hz	60	10000
7	6	10 Hz	60	100000

CAUTION

To remove knobs simply pry off the end button of the knob. Hold the knob firmly with your fingers or a padded tool and use a screwdriver to loosen the clutch device holding the knob to the shaft.

Do not loosen or tighten knob clutch by bearing against the end rotational stop of switches and potentiometers — always grasp the knob body firmly.

5-12. PACKING

The 5500A is a rugged instrument built to perform in severe environments. If the unit is to be shipped or stored for long periods of time the following packing procedure is recommended:

a) Place the 5500A into an oversize plastic bag and seal the bag.

b) Place the bagged 5500A into a heavy duty corrugated cardboard box. The box must contain at least 2 inches of rubberized hair or equivalent cushion on all six sides of the instrument. The counter must fit snugly into the cushion and the cushion must fit into the box to prevent any movement of the instrument in transit.

c) Place the instruction manual into the box. If accessories are also to be packed put them into a separate plastic bag and pack into the cushion leaving at least two inches of cushion between the instrument and the accessories as well as an extra cushion between accessories and the box.

d) Seal the box fully with 2 or 3 inch wide packing tape.

e) Properly label and address outside of box with a typed label or an indelible pen.

If shipment is to the factory, notify Ballantine in advance and include detailed reasons for return inside box along with your name, firm and full mailing address. Also include your phone number and purchase order number.

Ship prepaid by United Parcel Service or Registered Air Parcel Post to:

Ballantine Laboratories
90 Fanny Road
Post Office Box 97
Boonton, NJ USA 07055

Parts List

The replacement parts listed are available from the vendors listed or from Ballantine Labs. at the address shown above. Your local Ballantine Field Engineering Representative may also carry a stock of parts and can assist you. If pricing quotations are required for parts and or repairs your local representative will give the most rapid service or you may contact the Ballantine Factory directly.

When ordering replacement parts always give the following information:

a) Instrument Model number
b) Serial number
c) Ballantine Part number
d) Schematic Symbol number
e) Identification of the part

Ballantine will do its best to improve the instrument and make changes in style of components and replacement parts. Replacement parts may differ in appearance from those found in your instrument but are always equal or superior in performance. Where necessary minor mechanical modifications may be required in the replacement of components.

Parts are generally available locally for most replacements. The parts list calls out the recommended vendors where applicable.

The following parts coding are used:

CVC	Capacitor, Variable, Ceramic
CCT	Capacitor, Ceramic, Tubular
CFP	Capacitor, Fixed, Plastic
CCD	Capacitor, Ceramic, Disc
CYF	Capacitor, Mylar, Foil
CMD	Capacitor, Mica, Dipped
CMM	Capacitor, Mica, Molded
CEA	Capacitor, Electrolytic, Aluminum
CET	Capacitor, Electrolytic, Tantalum
DGP	Diode, General Purpose
DZG	Diode, Zener, General Purpose
DRP	Diode, Bridge, Power
FLT	Filter
ICP	Integrated Circuit
TRQ	Transistor
RFF	Resistor, Fixed, Film
RFC	Resistor, Fixed, Composition
RVC	Resistor, Variable, Composition
RFW	Resistor, Fixed, Wirewound
SWG	Switch
LMB	Lamp
TRX	Transformer

Resistors may generally be replaced by Corning Electronics (CGW) type N-55 and C-32. Allen Bradley composition resistors type EB are also used.

FRONT PANEL A1

SYMBOL	DESCRIPTION	MFR	BLI P/N
C1	CSM 0.002 uF/630 VDC	ST-TR	071-0005-0A
C2	CCD 4.7 pF	RMC	071-0006-0A
C3	CCD 47 pF	RMC	071-0007-0A
C4	CCD 470 pF	RMC	071-0008-0A
C5	CCD 1.5 nF	Sprague	070-2543-0A
C6	CSM 0.022 uF/630 VDC	ST-TR	071-0005-0A
C7	CCD 4.7 pF	RMC	071-0006-0A
C8	CCD 47 pF	RMC	071-0007-0A
C9	CCD 470 pF	RMC	071-0008-0A
C10	CCD 1.5 nF	Sprague	070-2543-0A
DS1	LMP MV 5023	H.P.	161-0000-0A
R1	RFC 5% 1/4W 1M	AB	121-2600-0A
R2	RFF 1% 1/4W 100k	CGW	121-2500-0A
R3	RFF 1% 1/4W 10k	CGW	121-2400-0A
R4	RFF 1% 1/4W 100k	CGW	121-2500-0A
R5	RFC 5% 1/4W 1M	AB	121-2600-0A
R6	RFF 1% 1/4W 100k	CGW	121-2500-0A
R7	RVC 1% 1/4W 10k	CGW	121-2400-0A
R8	RVC 1% 1/4W 100k	CGW	121-2500-0A
R9	Pot & SWC SPST 5k	BLI	094-0000-1A
R10	Pot & SWC SPST 5k	BLI	094-0000-1A
R11	Pot Log & SWC SPST 250k	BLI	094-0001-1A
S1	Switch Rotary dual Concentric	BLI	254-0020-0A
S2	Switch Rotary dual Concentric	BLI	254-0020-0A
S3	Part of R9	BLI	094-0001-1A
S4	Switch Slide DPDT	Stack	251-0022-0A
S5	Switch Slide DP3T	Stack	251-0021-0A
S6	Switch Slide DP3T	Stack	251-0021-0A
S7	Switch Slide DP3T	Stack	251-0021-0A
S8	Switch Slide DP3T	Stack	251-0021-0A
S9	Switch Slide DPDT	Stack	251-0022-0A
S10	Part of R10	BLI	094-0000-1A
S11	Switch Pushbutton SPST	Gray	251-0002-0A
S12	Part of R11	BLI	094-0001-1A
S13	Switch Slide DP3T	Stack	251-0021-0A

REAR PANEL A2

F1	Fuse 0.5A 3AG SLO-BLO	Buss.	190-3411-0A
J1	Connector BNC		
J2	Connector 50 pin 57-40500	Amph.	310-9513-0A
J3-1	Banana Post Red		
J3-2	Banana Post Black		
J3	Connector 24 pin 57-40240	Amph.	310-9511-0A
J4	Receptacle AC POW	Switcheft	311-0000-0A
S1	Switch Slide DPDT	Stack	250-7786-0A
S2	Switch Slide DPDT	Stack	251-0022-0A
S3	Switch Slide DPDT	Stack	250-7786-0A
T1	Transformer Power Assy.	BLI	204-0005-0A
TP1	Teflon Terminal Feed-Thru		
TP2	Teflon Terminal Feed-Thru		
TP3	Teflon Terminal Feed-Thru		
FL1	Line Surge Suppressor 150V	GE	141-0000-0A

MOTHERBOARD A3

SYMBOL	DESCRIPTION	MFR	BLI P/N
C1	CCD 150 pF 500 V	RMC	070-9575-0A
C2	CCD 1 nF 160 V	RMC	070-9561-0A
C3	CCT 10 uF/35 V	Sprague	071-0053-0A
C4	Capacitor, Trim. 7÷25 pF	Erie	071-0082-0A
C5	CMD 24 pF (typical)	ARCO	071-0011-0A
C6	CMD 100 pF	ARCO	071-0012-0A
C7	CMD 390 pF	ARCO	071-0253-0A
C8	CCD 22 nF 160 V	Sprague	070-2355-0A
C9	CCT 1.5 uF/35 V	Sprague	071-0083-0A
C10	CCD 22 nF 160 V	Sprague	070-2355-0A
C11	CCD 220 pF	RMC	070-9575-0A
C12	CCD 0.1 uF 50V	RMC	071-0082-0A
C13	CEA 50 uF/10 V	Sprague	070-7816-0A
C14	CCD 22 nF 160 V	RMC	070-2355-0A
C15	CCD 1 nF 500 V	RMC	070-9561-0A
C16	CCD 1 nF 500 V	RMC	070-9561-0A
C17	CCD 470 pF 500 V	RMC	071-0008-0A
C18	CCD 150 pF 500 V	RMC	070-9559-0A
C19	CCD 150 pF 500 V	RMC	070-9559-0A
C20	CCD 22 nF	RMC	070-2355-0A
C21	CCD 22 nF	RMC	070-2355-0A
C22	CCD 22 nF	RMC	070-2355-0A
C23	CCD 22 nF	RMC	070-2355-0A
C24	CCD 22 nF	RMC	070-2355-0A
C25	CCD 22 nF	RMC	070-2355-0A
C26	CCD 22 nF	RMC	070-2355-0A
C27	CCD 22 nF	RMC	070-2355-0A
C28	CCD 22 nF	RMC	070-2355-0A
C29	CCD 22 nF	RMC	070-2355-0A
C30	CCD 22 nF	RMC	070-2355-0A
C31	CEA 100 uF/16 V	STT	071-0089-0A
C32	CCD 220 pF	RMC	070-9575-0A
C33	CCT 1.5 uF/35 V	Sprague	071-0083-0A
C34	CCD 22 nF	RMC	070-2355-0A
C35	CCT 10 uF/35V	Sprague	071-0053-0A
C36	CCD 4.7 nF	Sprague	071-0089-0A
C37	CCD 47 nF	Amprex	071-0090-0A
C38	CEA 470 uF/6.3 V	ST-TR	071-0091-0A
C39	CCD 0.1 uF	ARCO	071-0082-0A
C40	CCD 4.7 nF	RMC	071-0089-0A
C41	CCT 1.5 uF/35 V	ST-TR	071-0083-0A
C42	CEA 16 uF/400 V	Sprague	070-9354-0A
C43	CEA 470 uF/35 V	ST-TR	071-0092-0A
C44	CCD 1 nF	RMC	070-9561-0A
C45	CEA 100 uF/16 V	ST-TR	071-0093-0A
C46	CEA 2200 uF/16 V	ST-TR	071-0094-0A
C47	CEA 1000 uF/16 V	Amprex	070-7833-0A
C48	CEA 100 uF/16 V	ST-TR	071-0093-0A
C49	CEA 470 uF/6.3 V	ST-TR	071-0091-0A
C50	CCD 22 nF 160 V	RMC	070-2355-0A
C51	CCD 22 nF 160 V	RMC	070-2355-0A
C52	CCD 22 nF 160 V	RMC	070-2355-0A
C53	CCD 22 nF 160 V	RMC	070-2355-0A
C54	CCD 22 nF 160 V	RMC	070-2355-0A
C55	CCD 22 nF 160 V	RMC	070-2355-0A
C56	CCD 22 nF 160 V	RMC	070-2355-0A
C57	CCD 22 nF 160 V	RMC	070-2355-0A
C58	CCD 22 nF 160 V	RMC	070-2355-0A
C59	CCD 22 nF 160 V	RMC	070-2355-0A
C60	CCD 22 nF 160 V	RMC	070-2355-0A
C61	CCD 22 nF 160 V	RMC	070-2355-0A
C62	CEA 220 uF/35 V	ST-TR	071-0095-0A
C63	CCD 22 nF 160 V	RMC	070-2355-0A
C64	CEA 220 uF/35 V	ST-TR	071-0095-0A
C65	CCD 22 nF 160 V	RMC	070-2355-0A
C66	CCT 1.5 uF/35 V	Sprague	071-0083-0A
C67	CEA 100 uF/16 V	ST-TR	071-0093-0A
C68	CCD 22 nF	RMC	070-2355-0A
C69	Inter. Supp. Cap 0.1+2x0.05	ST-TR	171-0000-0A

MOTHERBOARD A3

SYMBOL	DESCRIPTION	MFR	BLI P/N
CR1	Diode Ger. 1N281		051-0025-0A
CR2	Diode Ger. 1N281		051-0025-0A
CR3	Diode Si. 1N4151	MOT	051-0026-0A
CR4	Diode Si. 1N4151	MOT	051-0026-0A
CR5	Diode Si. 1N4151	MOT	051-0026-0A
CR6	Rectifier 1N4005	MOT	050-9481-0A
CR7	Rectifier 1N4003	MOT	050-9491-0A
CR8	Rectifier 1N4003	MOT	050-9491-0A
CR9	Rectifier 1N4003	MOT	050-9491-0A
CR10	Rectifier 1N4003	MOT	050-9491-0A
CR11	Rectifier 1N4999	MOT	051-0027-0A
CR12	Rectifier 1N4999	MOT	051-0027-0A
J1	Connector P.C. 30 pin		
Q1	Transistor NPN 2N4124	MOT	101-0034-0A
Q2	Transistor NPN 2N4124	MOT	101-0034-0A
Q3	Transistor PNP 2N3640	MOT	100-7934-0A
Q4	Transistor PNP 2N3640	MOT	100-7934-0A
Q5	Transistor NPN 2N4124	MOT	101-0034-0A
Q6	Not Used		
Q7	Transistor NPN 2N4124	MOT	101-0034-0A
Q8	Transistor NPN 2N4124	MOT	101-0034-0A
Q9	Transistor UJT 2N4852	MOT	101-0036-0A
Q10	Transistor NPN 2N4124	MOT	101-0034-0A
Q11	Transistor PNP 2N4126	MOT	101-0035-0A
Q12	Transistor PNP 2N4126	MOT	101-0035-0A
Q13	Transistor PNP 2N4126	MOT	101-0035-0A
Q14	Transistor NPN 2N1613	MOT	101-0032-0A
Q15	Transistor PNP MJE 370	MOT	101-0010-0A
Q16	Transistor NPN MJE 520	MOT	101-0004-0A
Q17	Transistor NPN MJE 520	MOT	101-0004-0A
R1	RFF 1% 1/4W 4640	CGW	121-2364-0A
R2	RFF 1% 1/4W 4640	CGW	121-2364-0A
R3	RFF 1% 1/4W 215	CGW	121-2232-0A
R4	RFF 1% 1/4W 4640	CGW	121-2364-0A
R5	RFF 1% 1/4W 4640	CGW	121-2364-0A
R6	RFF 1% 1/4W 215	CGW	121-2232-0A
R7	RFF 1% 1/4W 1k	CGW	121-2300-0A
R8	RFF 1% 1/4W 100	CGW	121-2200-0A
R9	RFF 1% 1/4W 100k	CGW	121-2500-0A
R10	RFF 1% 1/4W 10	CGW	121-2100-0A
R11	RFF 1% 1/4W 4640	CGW	121-2364-0A
R12	RFF 1% 1/4W 3480	CGW	121-2352-0A
R13	RFF 1% 1/4W 10	CGW	121-2100-0A
R14	RFF 1% 1/4W 1k	CGW	121-2300-0A
R15	RFF 1% 1/4W 4640	CGW	121-2364-0A
R16	RFF 1% 1/4W 2150	CGW	121-2322-0A
R17	RFF 1% 1/4W 10k	CGW	121-2400-0A
R18	RFF 1% 1/4W 100	CGW	121-2200-0A
R19	RFF 1% 1/4W 34.8	CGW	121-2152-0A
R20	RFF 1% 1/4W 215	CGW	121-2232-0A
R21	RFF 1% 1/4W 4640	CGW	121-2364-0A
R22	RFF 1% 1/4W 1k	CGW	121-2300-0A
R23	RFF 1% 1/4W 1k	CGW	121-2300-0A
R24	RFF 1% 1/4W 4640	CGW	121-2364-0A
R25	RFF 1% 1/4W 4640	CGW	121-2364-0A
R26	RFF 1% 1/4W 383	CGW	121-2256-0A
R27	RFF 1% 1/4W 383	CGW	121-2256-0A
R28	RFF 1% 1/4W 4640	CGW	121-2364-0A
R29	RFF 1% 1/4W 4640	CGW	121-2364-0A
R30	RFF 1% 1/4W 4640	CGW	121-2364-0A
R31	RFF 1% 1/4W 4640	CGW	121-2364-0A
R32	RFF 1% 1/4W 4640	CGW	121-2364-0A
R33	RFF 1% 1/4W 4640	CGW	121-2364-0A
R34	RFF 1% 1/4W 4640	CGW	121-2364-0A
R35	RFF 1% 1/4W 4640	CGW	121-2364-0A
R36	RFF 1% 1/4W 4640	CGW	121-2364-0A
R37	RFF 1% 1/4W 4640	CGW	121-2364-0A

MOTHERBOARD A3

SYMBOL	DESCRIPTION	MFR	BLI P/N
R38	RFF 1% 1/4W 4640	CGW	121-2364-0A
R39	RFF 1% 1/4W 1k	CGW	121-2300-0A
R40	RFF 1% 1/4W 383	CGW	121-2256-0A
R41	RFF 1% 1/4W 4640	CGW	121-2364-0A
R42	RFF 1% 1/4W 4640	CGW	121-2364-0A
R43	RFF 1% 1/4W 383	CGW	121-2256-0A
R44	RFF 1% 1/4W 3480	CGW	121-2352-0A
R45	RFF 1% 1/4W 1k	CGW	121-2300-0A
R46	RFF 1% 1/4W 383	CGW	121-2256-0A
R47	RFF 1% 1/4W 4640	CGW	121-2364-0A
R48	RFF 1% 1/4W 1k	CGW	121-2300-0A
R49	RFF 1% 1/4W 1k	CGW	121-2300-0A
R48	RFF 1% 1/4W 1k	CGW	121-2300-0A
R50	RFF 1% 1/4W 10k	CGW	121-2400-0A
R51	RFF 1% 1/4W 34.8	CGW	121-2152-0A
R52	RFF 1% 1/4W 14.7k	CGW	121-2416-0A
R53	RFF 1% 1/4W 1k	CGW	121-2300-0A
R54	RFF 1% 1/4W 100	CGW	121-2200-0A
R55	RFF 1% 1/4W 4640	CGW	121-2364-0A
R56	RFF 1% 1/4W 4640	CGW	121-2364-0A
R57	RFF 1% 1/4W 383	CGW	121-2256-0A
R58	RFF 1% 1/4W 1k	CGW	121-2300-0A
R59	RFF 1% 1/4W 4640	CGW	121-2364-0A
R60	RFF 1% 1/4W 4640	CGW	121-2364-0A
R61	RFF 1% 1/4W 100	CGW	121-2200-0A
R62	RFF 1% 1/4W 147	CGW	121-2216-0A
R63	RFF 1% 1/2W 215k	CGW	121-2532-0A
R64	RFC 5% 1/2W 1 ohm	AB	120-1057-0A
R65	RFF 1% 1/4W 2610	CGW	121-2340-0A
R66	RFF 1% 1/4W 3480	CGW	121-2352-0A
R67	RFF Factory selected (+15 Volt P.S.)		
R68	RFF 1% 1/4W 1k	CGW	121-2300-0A
R69	RFF Factory selected (+5 Volt P.S.)		
R70	RFF 1% 1/4W 825	CGW	121-2288-0A
R71	RFF 1% 1/4W 3480	CGW	121-2352-0A
R72	RFF 1% 1/4W 2610	CGW	121-2340-0A
R73	RFF 1% 1/4W 2150	CGW	121-2332-0A
R74	RFF 1% 1/4W 3480	CGW	121-2352-0A
R75	RFF 1% 1/4W 4640	CGW	121-2364-0A
R76	RFF 1% 1/4W 2610	CGW	121-2340-0A
R77	RFF Factory selected (−15 Volt P.S.)		
R78	RFF 1% 1/4W 3480	CGW	121-2352-0A
R79	RFF 1% 1/4W 1k	CGW	121-2300-0A
R80	RFF 1% 1/4W 1k	CGW	121-2300-0A
R83	RFF 1% 1/4W 215	CGW	121-2232-0A
U1	IC, TTL 8280	SIGNET	241-0014-0A
U2	IC, TTL 7400	MOT	240-9407-0A
U3	IC, TTL 7400	MOT	240-9407-0A
U4	IC, TTL 7410	MOT	241-0017-0A
U5	IC, TTL 7473	MOT	240-9409-0A
U6	IC, TTL 7400	MOT	240-9407-0A
U7	Not Used		
U8	IC, TTL 7453	MOT	241-0020-0A
U9	IC, MECL 1035P	MOT	241-0038-0A
U10	IC, TTL 7400	MOT	240-9407-0A
U11	IC, TTL 9312	MOT	241-0024-0A
U12	IC, TTL 8280	SIGNET	241-0014-0A
U13	IC, TTL 7440	MOT	241-0018-0A
U14	IC, TTL 7400	MOT	240-9407-0A
U15	IC, TTL 7474	TI	241-0002-0A
U16	IC, TTL 7450	MOT	241-0019-0A
U17	IC, TTL 7400	MOT	240-9407-0A
U18	IC, TTL 7404	MOT	241-0016-0A
U19	IC, TTL 7410	MOT	241-0017-0A
U20	IC, TTL 7420	TI	240-9406-0A

SYMBOL	DESCRIPTION	MFR	BLI P/N
	MOTHERBOARD A3		
U21	IC, TTL 8280	SIGNET	241-0014-0A
U22	IC, TTL 8280	SIGNET	241-0014-0A
U23	IC, TTL 8280	SIGNET	241-0014-0A
U24	IC, TTL 8280	SIGNET	241-0014-0A
U25	IC, TTL 8280	SIGNET	241-0014-0A
U26	IC, TTL 8280	SIGNET	241-0014-0A
U27	IC, TTL 8280	SIGNET	241-0014-0A
U28	IC, TTL 7400	MOT	240-9407-0A
U29	IC, TTL 7400	MOT	240-9407-0A
U30	IC, TTL 7410	MOT	241-0017-0A
U31	IC, TTL 7450	MOT	241-0019-0A
U32	IC, TTL 7400	MOT	241-9407-0A
U33	IC, Volt Reg 723	Fairch	240-9421-0A
XY1	Crystal Oven	Klixon	421-0000-0A
Y	Crystal 10 MHz TO-5	ERC	044-0003-0A
	DISPLAY ASSEMBLY A4		
C1	CCD 2.2 nF	RMC	071-0009-0A
C2	CCD 470 pF	RMC	071-0008-0A
C3	CCT 10 uF/35 V	ST-TR	071-0053-0A
C4	CCD 22 nF	RMC	070-2355-0A
C5	CCD 22 nF	RMC	070-2355-0A
C6	CCD 22 nF	RMC	070-2355-0A
C7	CCD 22 nF	RMC	070-2355-0A
CR1	DRP Rectifier 1N4005	MOT	050-9481-0A
CR2	DRP Rectifier 1N4005	MOT	050-9481-0A
CR3	DRG Diode Ger 1N281	ITT	051-0025-0A
CR4	DRG Diode Ger 1N281	ITT	051-0025-0A
CR5	DRG Diode Ger 1N281	ITT	051-0025-0A
CR6	DRG Diode Ger 1N281	ITT	051-0025-0A
DS1	TBE Numeric Indicator Tube 5780S	Burroughs	211-0000-0A
DS2	TBE Numeric Indicator Tube 5780S	Burroughs	211-0000-0A
DS3	TBE Numeric Indicator Tube 5780S	Burroughs	211-0000-0A
DS4	TBE Numeric Indicator Tube 5780S	Burroughs	211-0000-0A
DS5	TBE Numeric Indicator Tube 5780S	Burroughs	211-0000-0A
DS6	TBE Numeric Indicator Tube 5780S	Burroughs	211-0000-0A
DS7	TBE Numeric Indicator Tube 5780S	Burroughs	211-0000-0A
J1	Connector P.C. 30 pin		
Q1	TRQ Transistor NPN 2N4124	MOT	101-0034-0A
Q2	TRQ Transistor NPN 2N4124	MOT	101-0034-0A
Q3	TRQ Transistor NPN 2N4124	MOT	101-0034-0A
Q4	TRQ Transistor NPN 2N4124	MOT	101-0034-0A
Q5	TRQ Transistor NPN 2N4124	MOT	101-0034-0A
Q6	TRQ Transistor NPN 2N4124	MOT	101-0034-0A
Q7	TRQ Transistor NPN 2N4124	MOT	101-0034-0A
Q8	TRQ Transistor NPN 2N4124	MOT	101-0034-0A
Q9	TRQ Transistor NPN 2N4124	MOT	101-0034-0A

SYMBOL	DESCRIPTION	MFR	BLI P/N
	DISPLAY ASSEMBLY A4		
Q10	TRQ Transistor NPN 2N4410	MOT	100-7949-0A
Q11	TRQ Transistor NPN 2N4410	MOT	100-7949-0A
Q12	TRQ Transistor NPN 2N4410	MOT	100-7949-0A
R1	RFF 1% 1/4W 21.5k	CGW	121-2432-0A
R2	RFF 1% 1/4W 21.5k	CGW	121-2432-0A
R3	RFF 1% 1/4W 21.5k	CGW	121-2432-0A
R4	RFF 1% 1/4W 21.5k	CGW	121-2432-0A
R5	RFF 1% 1/4W 21.5k	CGW	121-2432-0A
R6	RFF 1% 1/4W 21.5k	CGW	121-2432-0A
R7	RFF 1% 1/4W 21.5k	CGW	121-2432-0A
R8	RFF 1% 1/4W 2150	CGW	121-2332-0A
R9	RFF 1% 1/4W 2150	CGW	121-2332-0A
R10	RFF 1% 1/4W 2150	CGW	121-2332-0A
R11	RFF 1% 1/4W 2150	CGW	121-2332-0A
R12	RFF 1% 1/4W 2150	CGW	121-2332-0A
R13	RFF 1% 1/4W 2150	CGW	121-2332-0A
R14	RFF 1% 1/4W 2150	CGW	121-2332-0A
R15	RFF 1% 1/4W 2150	CGW	121-2332-0A
R16	RFF 1% 1/4W 2150	CGW	121-2332-0A
R17	RFF 1% 1/4W 2150	CGW	121-2332-0A
R18	RFF 1% 1/4W 2150	CGW	121-2332-0A
R19	RFF 1% 1/4W 2150	CGW	121-2332-0A
R20	RFF 1% 1/4W 2150	CGW	121-2332-0A
R21	RFF 1% 1/4W 2150	CGW	121-2332-0A
R22	RFF 1% 1/4W 2150	CGW	121-2332-0A
R23	RFF 1% 1/4W 2150	CGW	121-2332-0A
R24	RFF 1% 1/4W 2150	CGW	121-2332-0A
R25	RFF 1% 1/4W 2150	CGW	121-2332-0A
R26	RFF 1% 1/4W 2150	CGW	121-2332-0A
R27	RFF 1% 1/4W 2150	CGW	121-2332-0A
R28	RFF 1% 1/4W 2150	CGW	121-2332-0A
R29	RFF 1% 1/4W 2150	CGW	121-2332-0A
R30	RFF 1% 1/4W 2150	CGW	121-2332-0A
R31	RFF 1% 1/4W 2150	CGW	121-2332-0A
R32	RFF 1% 1/4W 2150	CGW	121-2332-0A
R33	RFF 1% 1/4W 2150	CGW	121-2332-0A
R34	RFF 1% 1/4W 2150	CGW	121-2332-0A
R35	RFF 1% 1/4W 2150	CGW	121-2332-0A
R36	RFF 1% 1/4W 1k	CGW	121-2300-0A
R37	RFF 1% 1/4W 383	CGW	121-2256-0A
R38	RFF 1% 1/4W 383	CGW	121-2256-0A
R39	RFF 1% 1/4W 4640	CGW	121-2364-0A
R40	RFF 1% 1/4W 4640	CGW	121-2364-0A
R41	RFF 1% 1/4W 4640	CGW	121-2364-0A
R42	RFF 1% 1/4W 4640	CGW	121-2364-0A
R43	RFF 1% 1/4W 4640	CGW	121-2364-0A
R44	RFF 1% 1/4W 4640	CGW	121-2364-0A
R45	RFF 1% 1/4W 4640	CGW	121-2364-0A
R46	RFF 1% 1/4W 4640	CGW	121-2364-0A
R47	RFF 1% 1/4W 4640	CGW	121-2364-0A
R48	RFF 1% 1/4W 3480	CGW	121-2352-0A
R49	RFF 1% 1/4W 3480	CGW	121-2352-0A
R50	RFF 1% 1/4W 3480	CGW	121-2352-0A
R51	RFF 1% 1/4W 4640	CGW	121-2364-0A
R52	RFF 1% 1/4W 681	CGW	121-2280-0A
R53	RFF 1% 1/4W 681	CGW	121-2280-0A
R54	RFF 1% 1/4W 681	CGW	121-2280-0A
R55	RFF 1% 1/4W 681	CGW	121-2280-0A
R56	RFF 1% 1/4W 681	CGW	121-2280-0A
R57	RFF 1% 1/4W 681	CGW	121-2280-0A
R58	RFF 1% 1/4W 681	CGW	121-2280-0A
R59	RFF 1% 1/4W 681	CGW	121-2280-0A
R60	RFF 1% 1/4W 681	CGW	121-2280-0A
R61	RFF 1% 1/4W 348	CGW	121-2252-0A

SYMBOL	DESCRIPTION	MFR	BLI P/N
	DISPLAY ASSEMBLY A4		
U1	IC, DTL 846	MOT	240-9410-0A
U2	IC, TTL 7430	MOT	240-9414-0A
U3	IC, TTL 7400	MOT	240-9407-0A
U4	IC, TTL 7404	MOT	241-0016-0A
U5	IC, TTL 7400	MOT	240-9410-0A
U6	IC, TTL 7453	MOT	241-0020-0A
U7	Not Used		
U8	IC, TTL 7475	TI	241-0015-0A
U9	IC, TTL 7400	MOT	240-9410-0A
U10	IC, TTL 9322	MOT	241-0024-0A
U11	IC, TTL 8290	SIGNET	241-0026-0A
U12	IC, TTL 8280	SIGNET	241-0014-0A
U13	IC, TTL 8280	SIGNET	241-0014-0A
U14	IC, TTL 8280	SIGNET	241-0014-0A
U15	IC, TTL 8280	SIGNET	241-0014-0A
U16	IC, TTL 8280	SIGNET	241-0014-0A
U17	Not Used		
U18	Not Used		
U19	IC, TTL 74145	TI	241-0022-0A
U20	IC, TTL 7400	MOT	240-9410-0A
U21	IC, DTL 936	MOT	241-0034-0A
U22	IC, TTL 7475	TI	241-0015-0A
U23	IC, TTL 7475	TI	241-0015-0A
U24	IC, TTL 7475	TI	241-0015-0A
U25	IC, TTL 7475	TI	241-0015-0A
U26	IC, TTL 7475	TI	241-0015-0A
U27	IC, TTL 7475	TI	241-0015-0A
U28	IC, TTL 7475	TI	241-0015-0A
U29	IC, TTL 7441	SIGNET	241-0013-0A
U30	IC, TTL 7441	SIGNET	241-0013-0A
U31	IC, TTL 7441	SIGNET	241-0014-0A
U32	IC, TTL 7441	SIGNET	241-0014-0A
U33	IC, TTL 7441	SIGNET	241-0014-0A
U34	IC, TTL 7441	SIGNET	241-0014-0A
U35	IC, TTL 7441	SIGNET	241-0014-0A
	INPUT ASSEMBLY A5		
C1	CCD 0.1 uF 50 V	RMC	071-0082-0A
C2	CCT 10 uF 35 V	Sprague	071-0053-0A
C3	CCT 1.5 uF 35 V	Sprague	071-0083-0A
C4	CCT 10 uF 35 V	Sprague	071-0053-0A
C5	CCD 0.1 uF 50 V	RMC	071-0082-0A
C6	CCD 0.01 uF 160 V	RMC	070-9009-0A
C7	CCD 22 nF 160 V	RMC	070-2355-0A
C8	CCD 22 nF 160 V	RMC	070-2355-0A
C9	CCT 1.5 uF 35 V	Sprague	071-0083-0A
C10	CCD 3.3 pF 500 V	RMC	071-0081-0A
C11	CCD 0.1 nF 50 V	RMC	071-0082-0A
C12	CCT 1.5 uF 35 V	Sprague	071-0083-0A
C13	CCD 22 nF 160 V	RMC	070-2355-0A
C14	CCD 22 nF 160 V	RMC	070-2355-0A
C15	CCD 22 pF 500 V	RMC	071-0085-0A
C16	CCT 10 uF 35 V	Sprague	071-0053-0A
C17	CCD 0.1 uF 50 V	RMC	071-0082-0A
C18	CCT 1.5 uF 35 V	Sprague	071-0083-0A
C19	CCD 68 pF 500 V	RMC	071-0086-0A
C20	CCD 220 pF 600 V	RMC	070-9575-0A
C21	CCT 1.5 uF 35 V	Sprague	071-0083-0A
C22	CCD 33 pF 500 V	RMC	070-9560-0A
C23	CCT 1.5 uF 35 V	Sprague	071-0083-0A
C24	CCT 1.5 uF 35 V	Sprague	071-0083-0A
C25	CCD 0.01 uF 160 V	RMC	070-9009-0A
C26	CCD 22 nF 160 V	RMC	070-2355-0A
C27	CCD 22 nF 160 V	RMC	070-2355-0A
C28	CCT 1.5 uF 35 V	Sprague	071-0083-0A
C29	CCT 1.5 uF 35 V	Sprague	071-0083-0A
CR1	Diode, Hot Carrier HP-2800	H.P.	050-9462-0A
CR2	Diode, Hot Carrier HP-2800	H.P.	050-9462-0A

SYMBOL	DESCRIPTION	MFR	BLI P/N
	INPUT ASSEMBLY A5		
CR3	Diode, Zener 1N756 (8,2 V)	MOT	050-0494-0A
CR4	Diode, Zener 1N750 (4,7 V)	MOT	051-1001-0A
CR5	Diode, Zener 1N753 (6,2 V)	MOT	051-1000-0A
CR6	Diode, Germanium 1N281	ITT	051-0025-0A
CR7	Diode, Germanium 1N281	ITT	051-0025-0A
CR8	Diode, Silieon 1N4151	MOT	051-0026-0A
CR9	Diode, Silieon 1N4151	MOT	051-0026-0A
CR10	Diode, Zener 1N746 (3,3 V)	MOT	051-0017-0A
CR11	Diode, Zener 1N753 (6,2 V)	MOT	051-0000-0A
CR12	Diode, Hot Carrier HP-2800	H.P.	050-9462-0A
L1	Ferrite Bead Ceramag 24	Stackpole	461-0003-0A
L2	Ferrite Bead Ceramag 7D	Stackpole	461-0004-0A
Q1	FET (Dual) UC-2149	U.C.	101-0039-0A
Q2	Transistor NPN 2N5179	MOT	101-0037-0A
Q3	Transistor NPN 2N5179	MOT	101-0037-0A
Q4	Transistor NPN 2N4124	MOT	101-0034-0A
Q5	Transistor NPN 2N4124	MOT	101-0034-0A
Q6	Transistor PNP 2N4126	MOT	101-0035-0A
Q7	Transistor NPN 2N3646	MOT	101-0033-0A
Q8	Transistor NPN 2N3646	MOT	101-0033-0A
Q9	Transistor NPN 2N5179	MOT	101-0037-0A
Q10	Transistor NPN 2N5179	MOT	101-0037-0A
Q11	Transistor NPN 2N5179	MOT	101-0037-0A
Q12	FET (Dual) UC-2149	U.C.	101-0039-0A
Q13	Transistor PNP 2N4126	MOT	101-0035-0A
Q14	Transistor PNP 2N4126	MOT	101-0035-0A
Q15	Transistor NPN 2N3646	MOT	101-0033-0A
R1	RFF 1% 1/4W 46.4	CGW	121-2164-0A
R2	RFF 1% 1/4W 10k	CGW	121-2400-0A
R3	RFC 5% 1/8W 33	AB	121-2703-0A
R4	RFF 1% 1/4W 2150	CGW	121-2332-0A
R5	RFF 1% 1/4W 2150	CGW	121-2332-0A
R6	RVC 1k	Bourns	091-0045-0A
R7	RFC 1% 1/4W 46.4	CGW	121-2164-0A
R8	RFF 1% 1/4W 38.3	CGW	121-2156-0A
R9	RFC 5% 1/8W 33	AB	121-2703-0A
R10	RFF 1% 1/4W 10k	CGW	121-2400-0A
R11	RFF 1% 1/4W 1470	CGW	121-2316-0A
R12	RFC 5% 1/4W 1M	AB	121-2600-0A
R13	RFC 1% 1/4W 4640	CGW	121-2364-0A
R14	RFC 1% 1/4W 562	CGW	121-2272-0A
R15	RFC 1% 1/4W 4640	CGW	121-2364-0A
R16	RFC 1% 1/4W 567	CGW	121-2272-0A
R17	RVC 1% 1/4W 500	Bourns	091-0044-0A
R18	RFF 1/ 1/4W 681	CGW	121-2280-0A
E19	RFF 1% 1/4W 562	CGW	121-2272-0A
R20	RFF 1% 1/4W 681	CGW	121-2280-0A
R21	RFC 5% 1/8W 220	AB	121-2710-0A
R22	RFF 1% 1/4W 1210	CGW	121-2308-0A
R23	RFC 5% 1/8W 27	AB	121-2702-0A
R24	RFF 1% 1/4W 100	CGW	121-2200-0A
R25	RFF 1% 1/4W 3480	CGW	121-2352-0A
R26	RFF 1% 1/4W 348	CGW	121-2252-0A
R27	RFC 5% 1/8W 27	AB	121-2702-0A
R28	RFC 1% 1/4W 1780	CGW	121-2324-0A
R29	RFC 5% 1/8W 10	AB	121-2700-0A
R30	RFF 1% 1/4W 26.1	CGW	121-2140-0A
R31	RFF 1% 1/4W 261	CGW	121-2240-0A
R32	RFF 1% 1/4W 1k	CGW	121-2300-0A
R33	RFF 1% 1/4W 562	CGW	121-2272-0A
R34	RFF 1% 1/4W 2610	CGW	121-2340-0A
R35	RFF 1% 1/4W 1210	CGW	121-2308-0A
R36	RFF 1% 1/4W 1k	CGW	121-2300-0A
R37	RFF 1% 1/4W 348	CGW	121-2252-0A
R38	RFF 1% 1/4W 215	CGW	121-2232-0A
R39	RFF 1% 1/4W 1470	CGW	121-2316-0A
R40	RFF 1% 1/4W 1k	CGW	121-2300-0A

INPUT ASSEMBLY A5

SYMBOL	DESCRIPTION	MFR	BLI P/N
R41	RFF 1% 1/4W 464	CGW	121-2264-0A
R42	RFF 1% 1/4W 464	CGW	121-2264-0A
R43	RFF 1% 1/4W 46.4	CGW	121-2164-0A
R44	RFF 1% 1/4W 215	CGW	121-2232-0A
R45	RFF 1% 1/4W 215	CGW	121-2332-0A
R46	RFF 1% 1/4W 215	CGW	121-2332-0A
R47	RFF 1% 1/4W 46.4	CGW	121-2164-0A
R48	RFF 1% 1/4W 681	CGW	121-2280-0A
R49	RVC 1% 1/4W 1k	Bourns	091-0045-0A
R50	RFC 5% 1/8W 220	AB	121-2710-0A
R51	RFC 5% 1/8W 220	AB	121-2710-0A
R52	RFC 5% 1/8W 68	AB	121-2707-0A
R53	RFC 5% 1/8W 68	AB	121-2707-0A
R54	RFF 1% 1/4W 1470	CGW	121-2316-0A
R55	RFF 1% 1/4W 100	CGW	121-2200-0A
R56	RFF 1% 1/4W 687	CGW	121-2280-0A
R57	RFF 1% 1/4W 100	CGW	121-2200-0A
R58	RFC 5% 1/4W 1M	AB	121-2600-0A
R59	RFF 1% 1/4W 4640	CGW	121-2364-0A
R60	RFF 1% 1/4W 562	CGW	121-2272-0A
R61	RFF 1% 1/4W 562	CGW	121-2272-0A
R62	RFF 1% 1/4W 4640	CGW	121-2364-0A
R63	RFF 1% 1/4W 215	CGW	121-2232-0A
R64	RFF 1% 1/4W 215	CGW	121-2232-0A
R65	RFF 1% 1/4W 14.7k	CGW	121-2416-0A
R66	RFF 1% 1/4W 3830	CGW	121-2356-0A
R67	RFF 1% 1/4W 464	CGW	121-2264-0A
U1	IC, TTL (Schottky) 74S00	TI	241-0030-0A
U2	IC, TTL (Schottky) 74S112	TI	241-0032-0A
U3	IC, TTL (Schottky) 74S112	TI	241-0032-0A
U4	IC, Comparator 710	Fairch	241-0040-0A

MISCELLANEOUS

SYMBOL	DESCRIPTION	MFR	BLI P/N
	P.C. Interconnection (A7)	BLI	314-0051-1A
	FLT Polaroid Window Filter	BLI	474-0001-1A
	Cord AC Power 7 ft.	BLI	331-0000-0A
	Pointer 10 mm BLK	BLI	401-0002-0A
	KNB 10 mm BLK 1/8" Shaft	BLI	401-0003-0A
	Cap 10 mm BLK	BLI	401-0004-0A
	KNB 14.5 mm BLK 3mm Shaft	BLI	401-0005-0A
	Cap 14.5 mm RED	BLI	401-0006-0A
	KNB 23 mm BLK 6mm Shaft	BLI	401-0007-0A
	FLT Film Screen, Annunciator	BLI	474-0002-1A
DS1	LMP Lamp Incadescent	SYL	161-0005-0A
DS2	LMP Lamp Incadescent	SYL	161-0005-0A
DS3	LMP Lamp Incadescent	SYL	161-0005-0A
DS4	LMP Lamp Incadescent	SYL	161-0005-0A
DS5	LMP Lamp Incadescent	SYL	161-0005-0A
DS6	LMP Lamp Incadescent	SYL	161-0005-0A

Circuit Diagrams

This section contains component location illustrations and schematics for the 5500A. The component location illustrations identify, by reference designation, the location of all components shown on the schematics.

All the components shown on the schematics and component location illustrations are described in the parts list in Section 6. Any replacement parts required should be selected from the parts list.

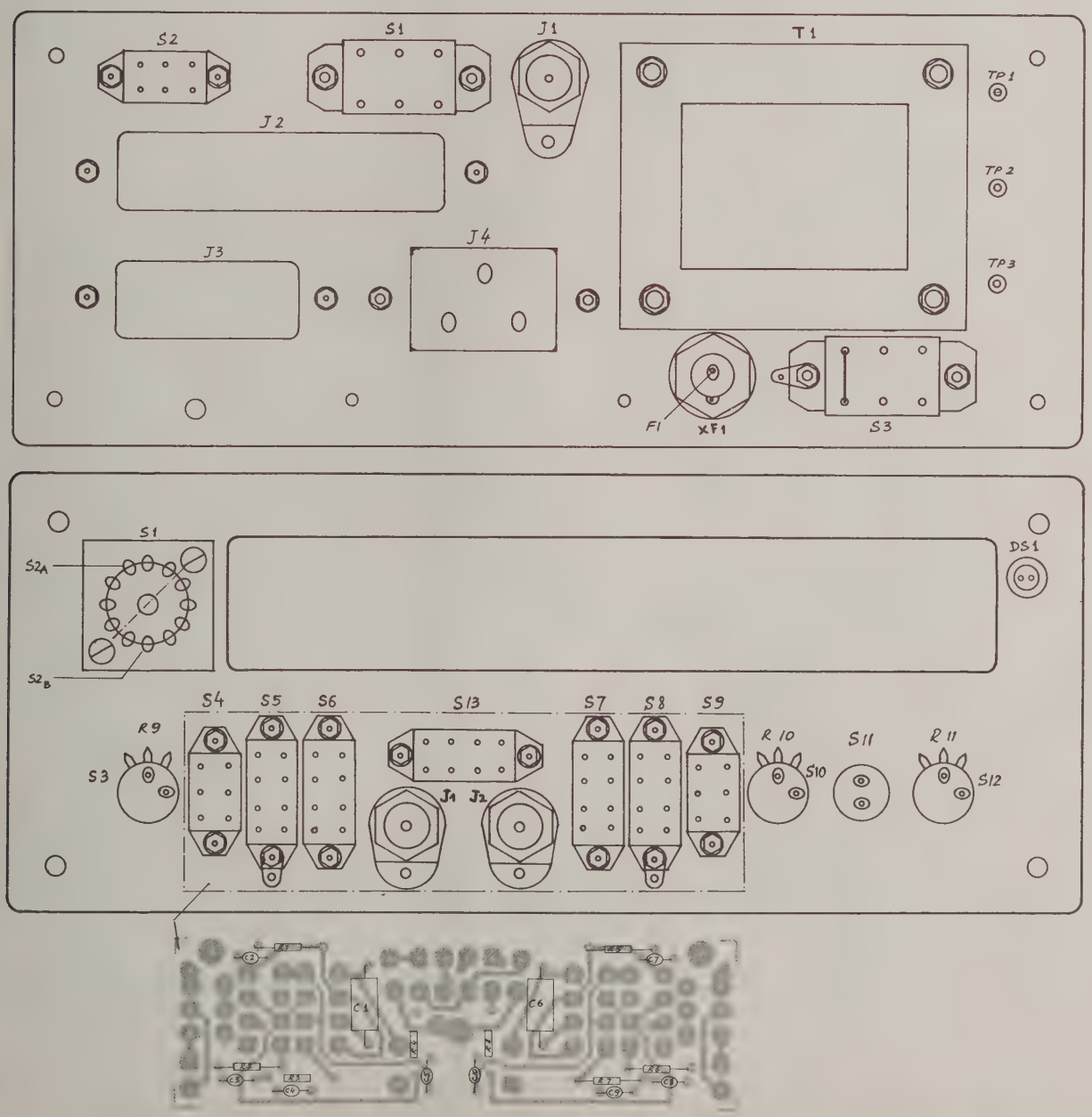


FIGURE 7-1. COMPONENT LOCATIONS, FRONT PANEL A1 & REAR PANEL A2

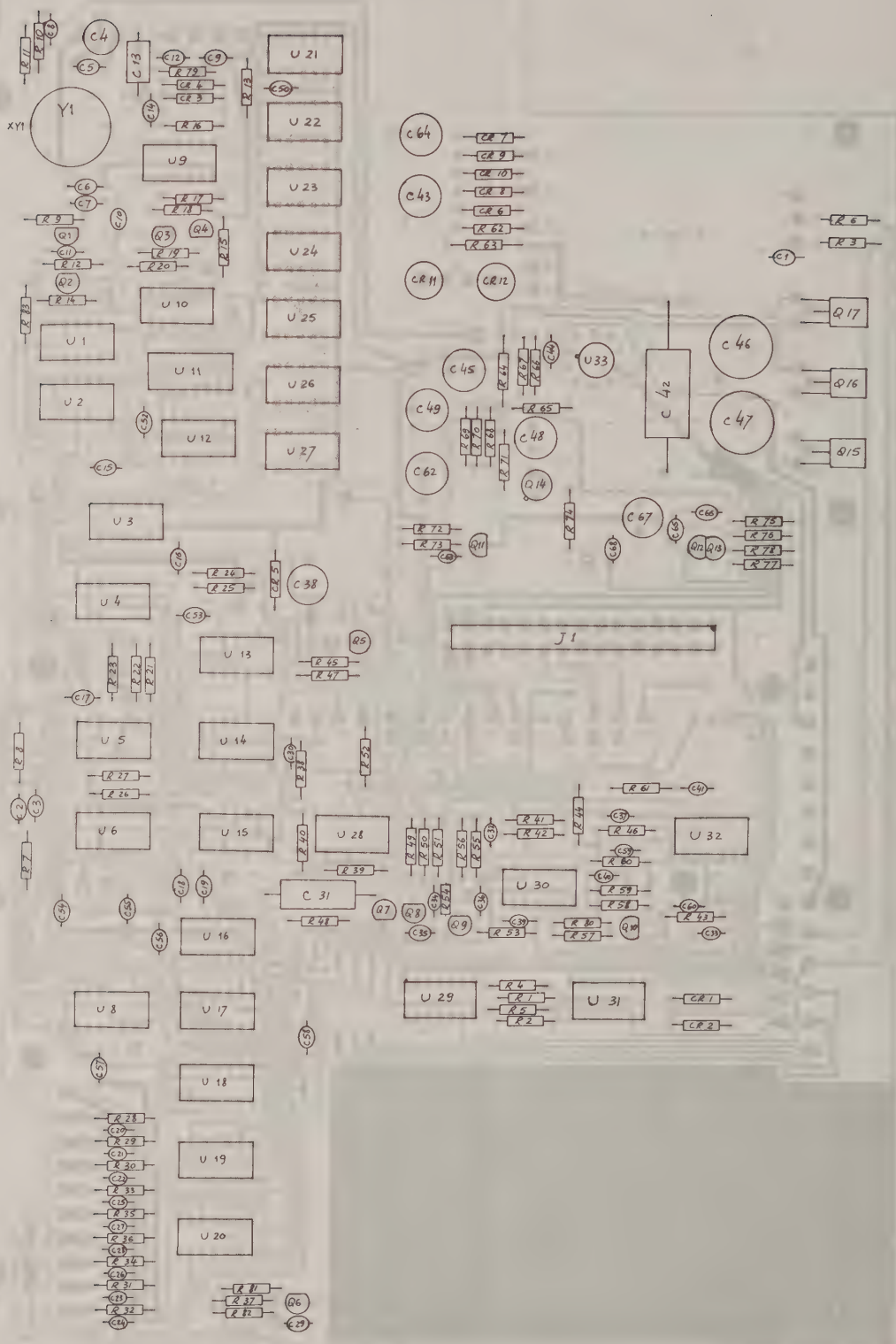
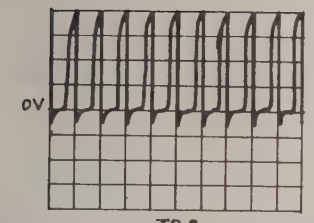
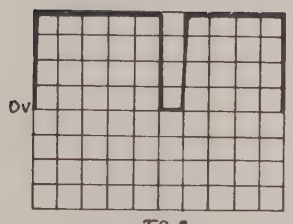


FIGURE 7-2. COMPONENT LOCATIONS, MOTHERBOARD A3



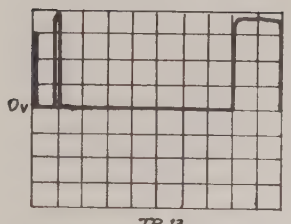
TP 2

.1 V/cm
.1 μS/cm



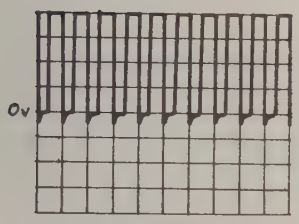
TP 8

RESOLUTION - - - - - 1 SEC
.1 V/cm
.2 Sec/cm



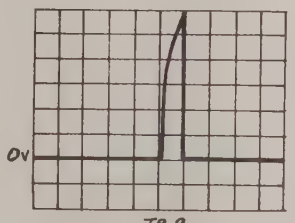
TP 13

.1 V/cm
.1 mS/cm



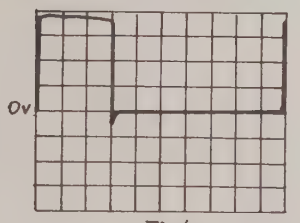
TP 3

.1 V/cm
.1 μS/cm



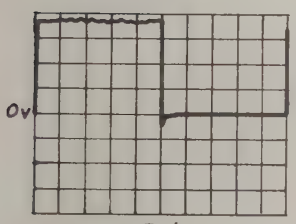
TP 9

RESOLUTION - - - - 1 SEC
.2 V/cm
.2 Sec/cm



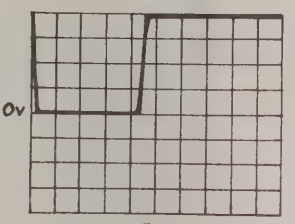
TP 14

.1 V/cm
.1 μS/cm



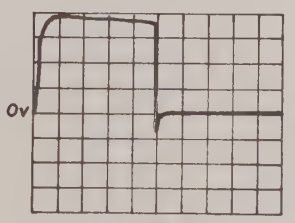
TP 4

.1 V/cm
.1 μS/cm



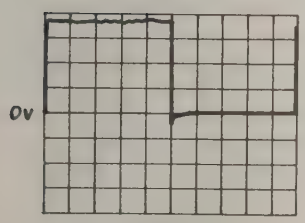
TP 10

.1 V/cm
20 μS/cm



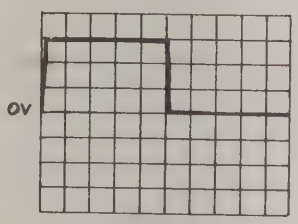
TP 15

.1 V/cm
.1 μS/cm



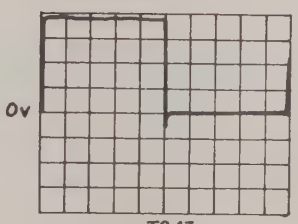
TP 5

RESOLUTION - - - - - .1 SEC
.1 V/cm
.1 μS/cm



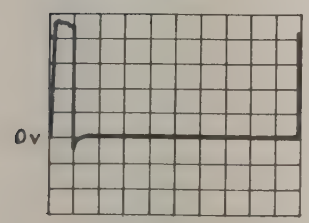
TP 11

STORAGE - - - - - ON
.1 V/cm
5 μS/cm



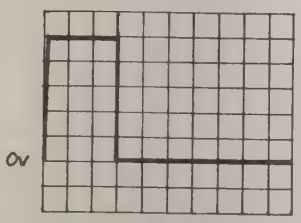
TP 17

FUNCTION - - - ⊓
.1 V/cm
.1 μS/cm



TP 7

.1 V/cm
.1 μS/cm



TP 12

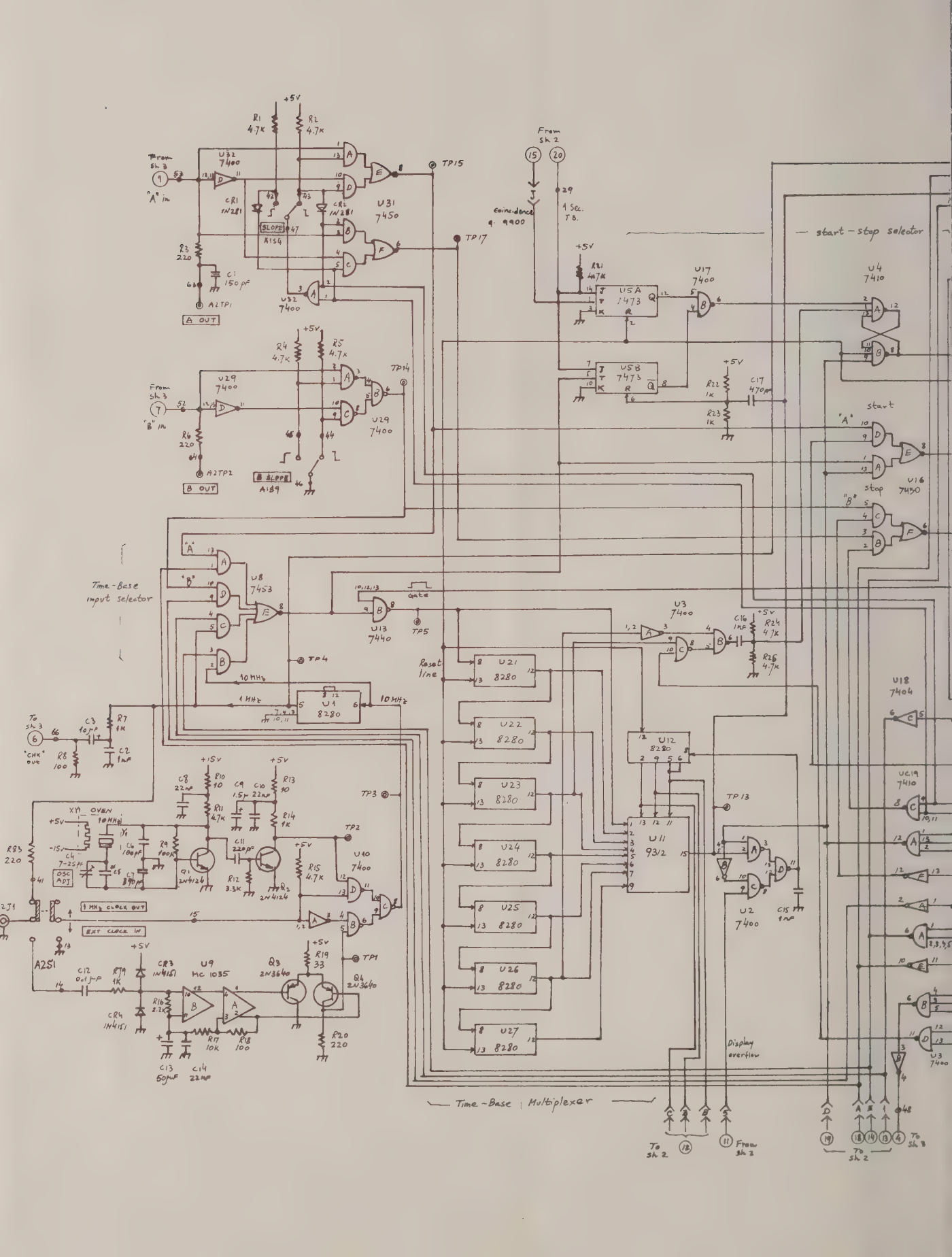
.1 V/cm
.2 mS/cm

All waveforms dc coupled through 10:1 divider probe.

Counter Controls unless otherwise specified:

SEP/COM/CHK	CHK
FUNCTION	FREQ
RESOLUTION	4
DISPLAY TIME	min

FIGURE 7-3. TEST POINT WAVEFORMS, MOTHERBOARD A3


start - stop selector
Time-Base input selector
Time - Base | Multiplexer
Display overflow
start
stop
Reset line
Gate
10 MHz
1 MHz
1 MHz CLOCK OUT
EXT CLOCK IN
OSC ADJ
SLOPE
A OUT
B OUT
A2TP1
A2TP2
A2S1
From Sh 3
From Sh 2
To Sh 2
To Sh 3
1 Sec. TB.
Coincidence 9900
"A" in
"B" in
"CHK" out
U1 8280
U2 7400
U3 7400
U4 7410
U8 7453
U9 MC 1035
U10 7400
U11 93/2
U12 8280
U13 7440
U16 7450
U17 7400
U18 7404
U19 7410
U21 8280
U22 8280
U23 8280
U24 8280
U25 8280
U26 8280
U27 8280
U29 7400
U31 7450
U32 7400
U5A 7473
U5B 7473
TP1
TP2
TP3
TP4
TP5
TP13
TP14
TP15
TP17

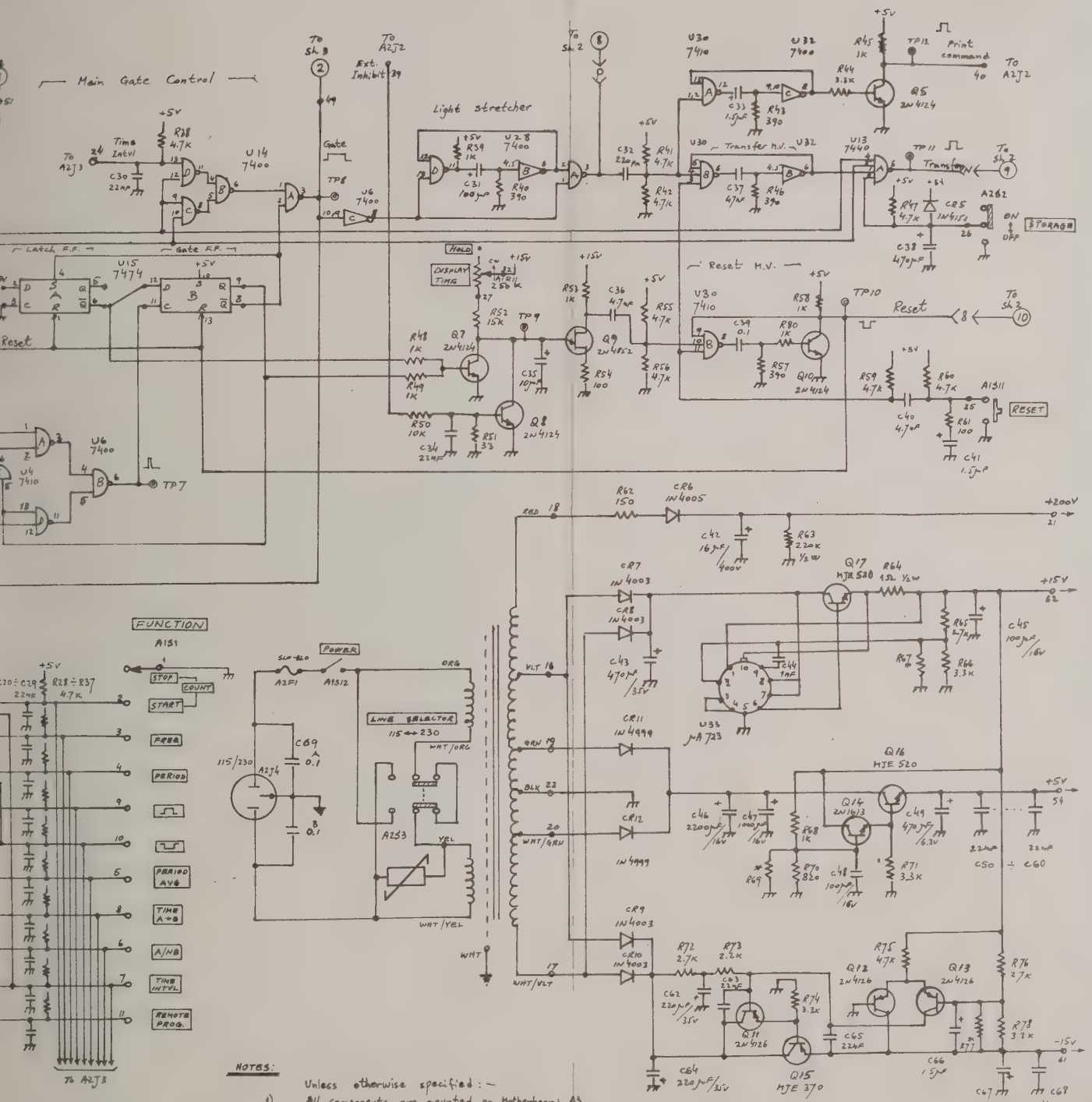


FIGURE 7-4. SCHEMATIC, MOTHERBOARD A3

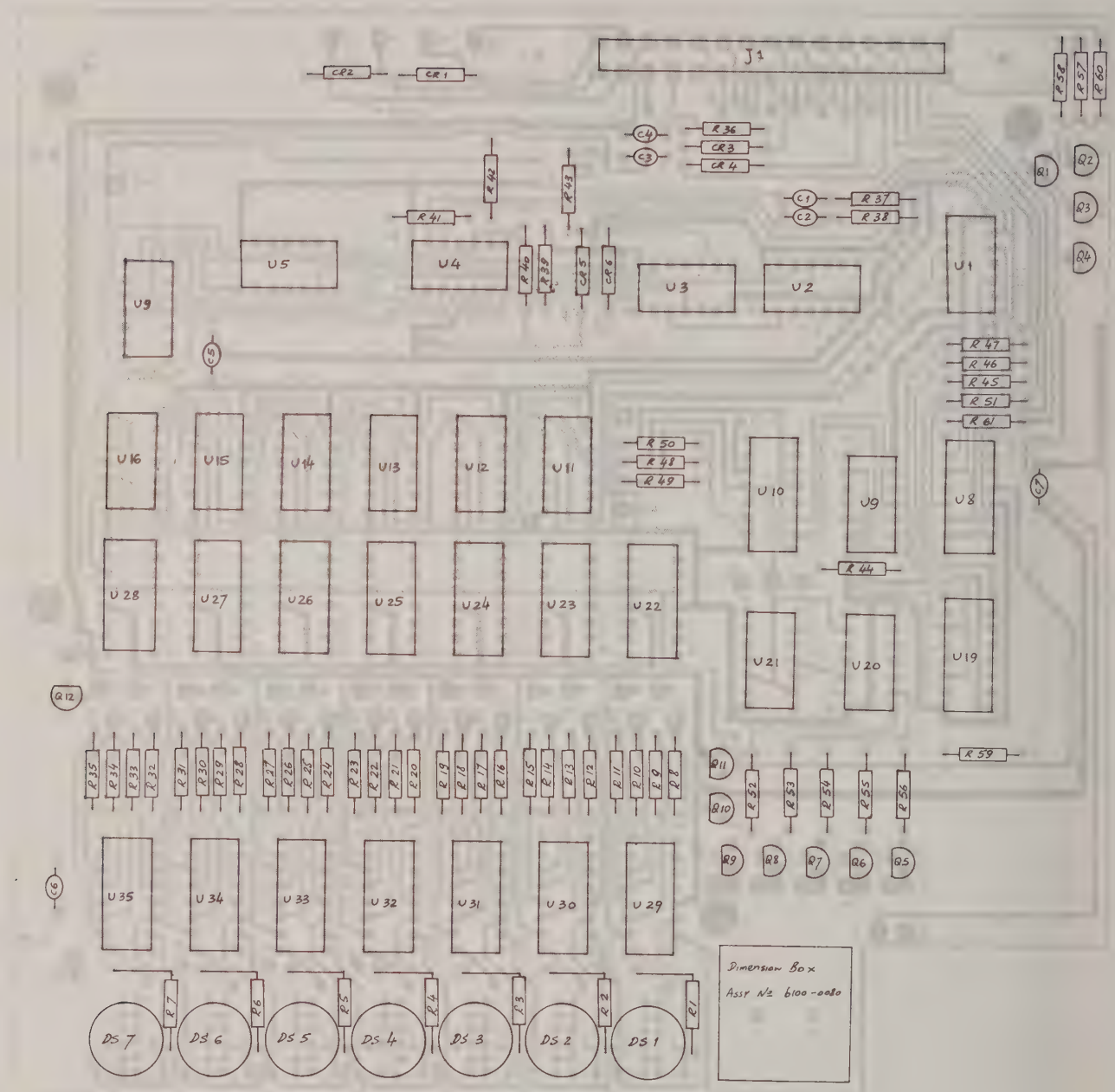
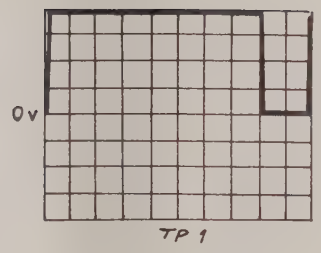
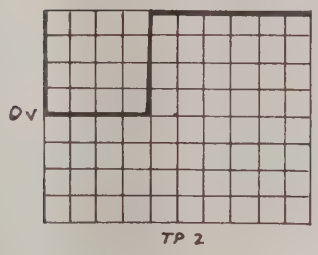
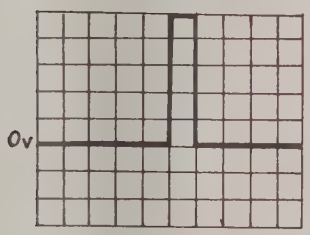
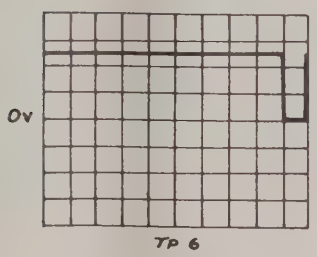


FIGURE 7-5. COMPONENT LOCATIONS, DISPLAY ASSEMBLY A4







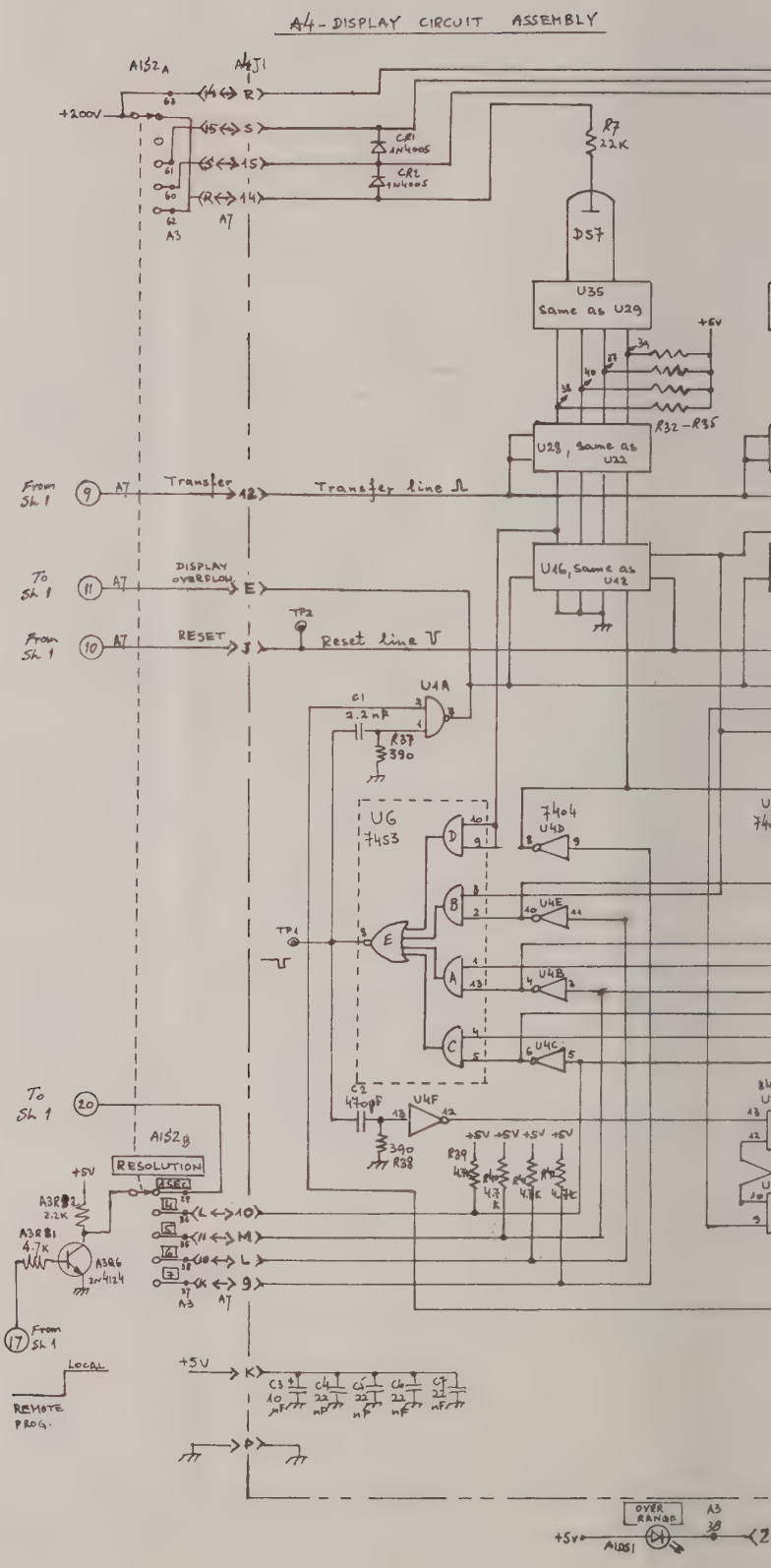


All waveforms dc coupled through 10:1 divider probe.

Counter Controls unless otherwise specified:

SEP/COM/CHK . . . . . CHK
FUNCTION . . . . . FREQ
RESOLUTION 4
TRIG LEVEL . . . . . PSET
DISPLAY TIME . . . . . min

FIGURE 7-6. TEST POINT WAVEFORMS, DISPLAY ASSEMBLY A4


A4 - DISPLAY CIRCUIT ASSEMBLY
A1S2A
A4J1
+200V
CR1 1N4005
CR2 1N4005
R7 22K
DS7
U35 same as U29
+5V
R32 - R35
U29, same as U22
From Sh 1
Transfer
Transfer line N
To Sh 1
DISPLAY OVERFLOW
From Sh 1
RESET
Reset line V
TP2
U1A
C1 2.2 nF
R37 390
U6 7453
7404 U4D
U4E
U4B
U4C
TP1
C2 470pF
U4F
R38 390
R39 R40 R41 R42 4.7K
To Sh 1
A1S2B
RESOLUTION
+5V
A3R82 2.2K
A3R81 4.7K
A3Q6 2N4124
From Sh 1
LOCAL
REMOTE PROG.
+5V
C3 10 µF
C4 C5 C6 C7 22 nF
OVER RANGE
A3
+5V
A1DS1

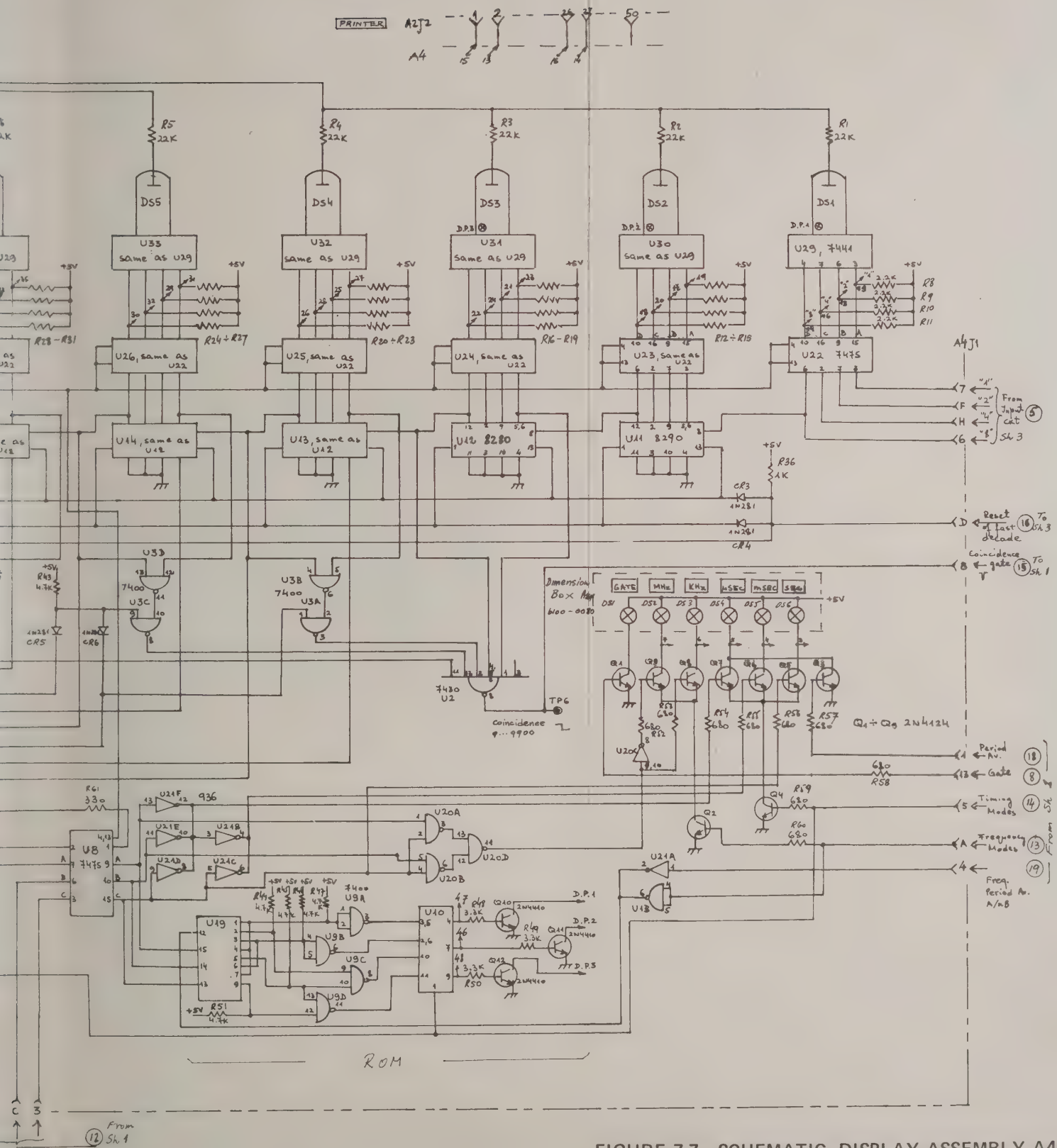


FIGURE 7-7. SCHEMATIC, DISPLAY ASSEMBLY A4

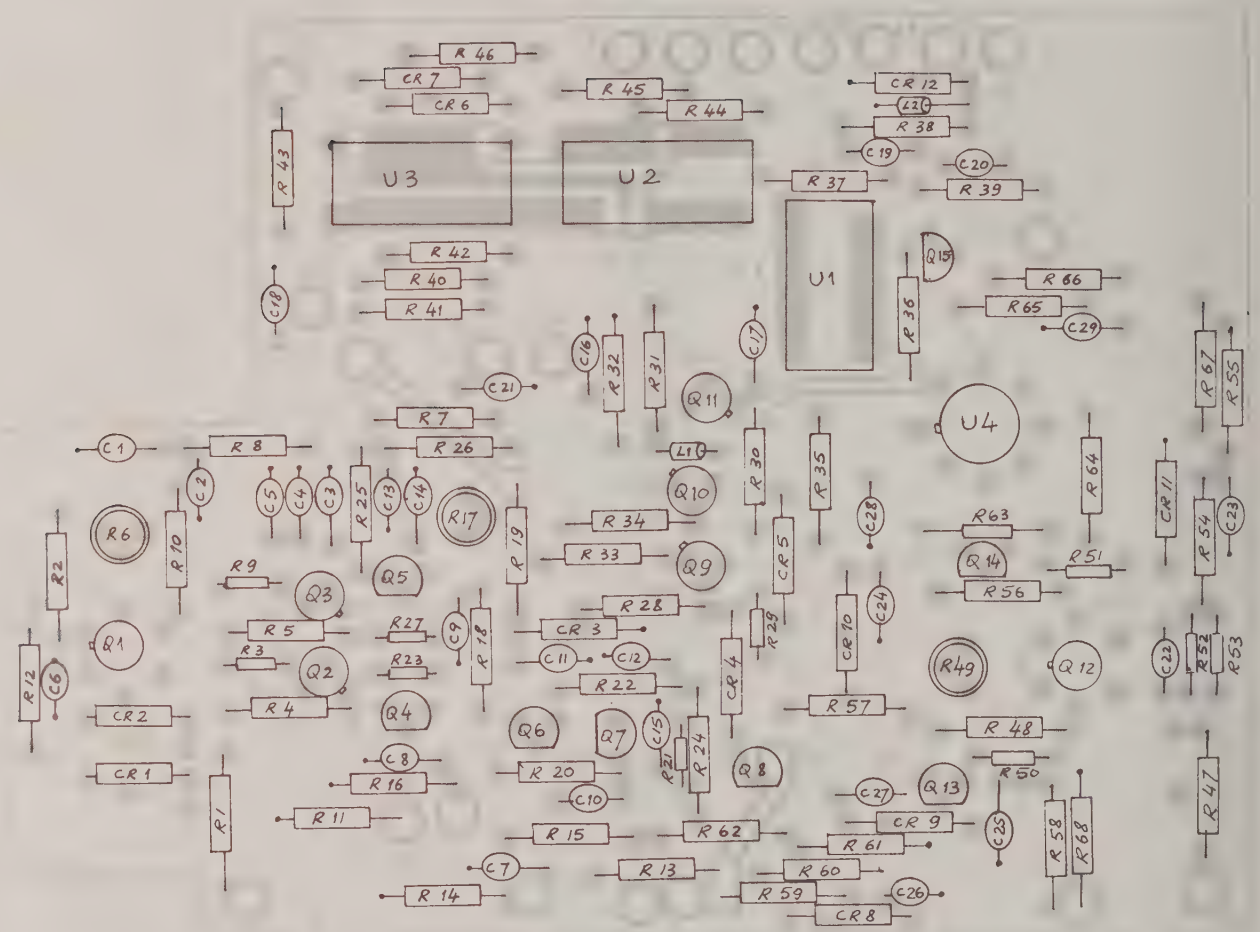
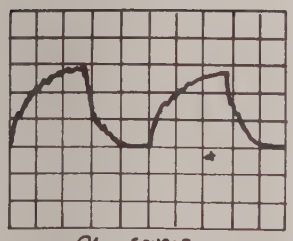
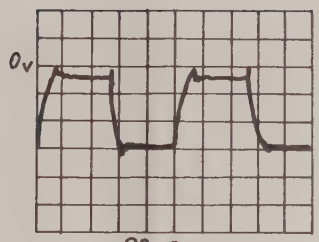


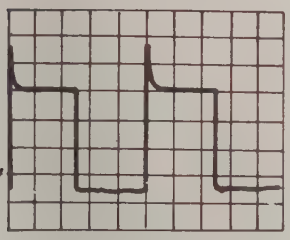
FIGURE 7-8. COMPONENT LOCATIONS, INPUT CIRCUIT A5



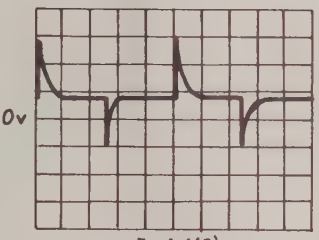
$Q1_A$ SOURCE
divider probe .... AC coupled
.01 V/cm
.2 μS/cm



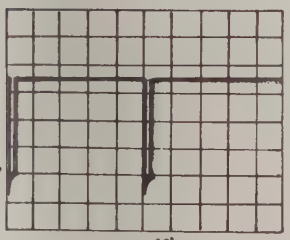
Q9 BASE
.1 V/cm
.2 μS/cm



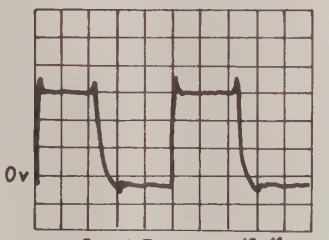
IC 1 (2)
.1 V/cm
.2 μS/cm



IC 1 (10)
.1 V/cm
.2 μS/cm



IC 1 (8)
.1 V/cm
.2 μS/cm



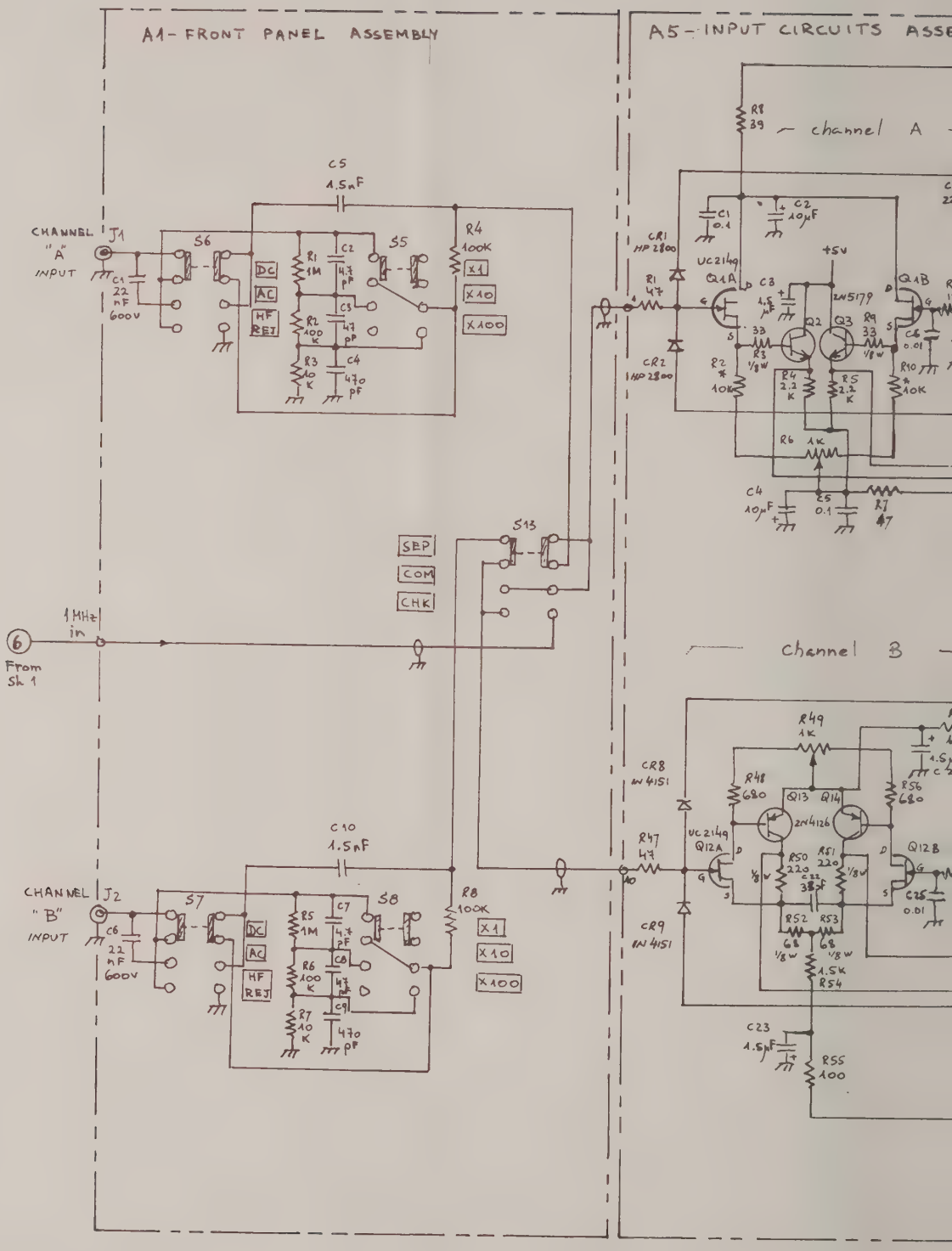
WIRE TIE POINT NR 11
.1 V/cm
.2 μS/cm

All waveforms dc coupled through 10:1 divider probe.

Counter Controls unless otherwise specified:

SEP/COM/CHK . . . . . CHK
FUNCTION . . . . . FREQ
RESOLUTION 4
TRIG LEVEL . . . . . PSET
DISPLAY TIME . . . . . min

FIGURE 7-9. TEST POINT WAVEFORMS, INPUT CIRCUIT A5


A1- FRONT PANEL ASSEMBLY
A5- INPUT CIRCUITS ASSE
CHANNEL "A" INPUT
J1
S6
S5
C5 1.5nF
R4 100K
DC
AC
HF REJ
X1
X10
X100
C1 22 nF 600V
R1 1M
C2 47 pF
R2 100 K
C3 47 pF
R3 10 K
C4 470 pF
S13
SEP
COM
CHK
1 MHz in
6
From Sk 1
channel A
channel B
R8 39
C1 0.1
C2 10µF
CR1 HP 2800
CR2 HP 2800
UC2149
Q1A
Q1B
C3 4.5 µF
2N5179
Q2
Q3
R9 33
C6 0.01
R3 33
R2 10K
R4 2.2 K
R5 2.2 K
R10 10K
R6 1K
C4 10µF
C5 0.1
R7 47
R49 1K
CR8 IN 4151
CR9 IN 4151
R48 680
R56 680
Q13
Q14
2N4126
R47 47
Q12A
Q12B
R50 220
R51 220
C22 33pF
C25 0.01
R52 68
R53 68
R54 1.5K
C23 1.5µF
R55 100
CHANNEL "B" INPUT
J2
S7
S8
C10 1.5nF
R8 100K
C6 22 nF 600V
R5 1M
C7 47 pF
R6 100 K
C8 47 pF
R7 10 K
C9 470 pF

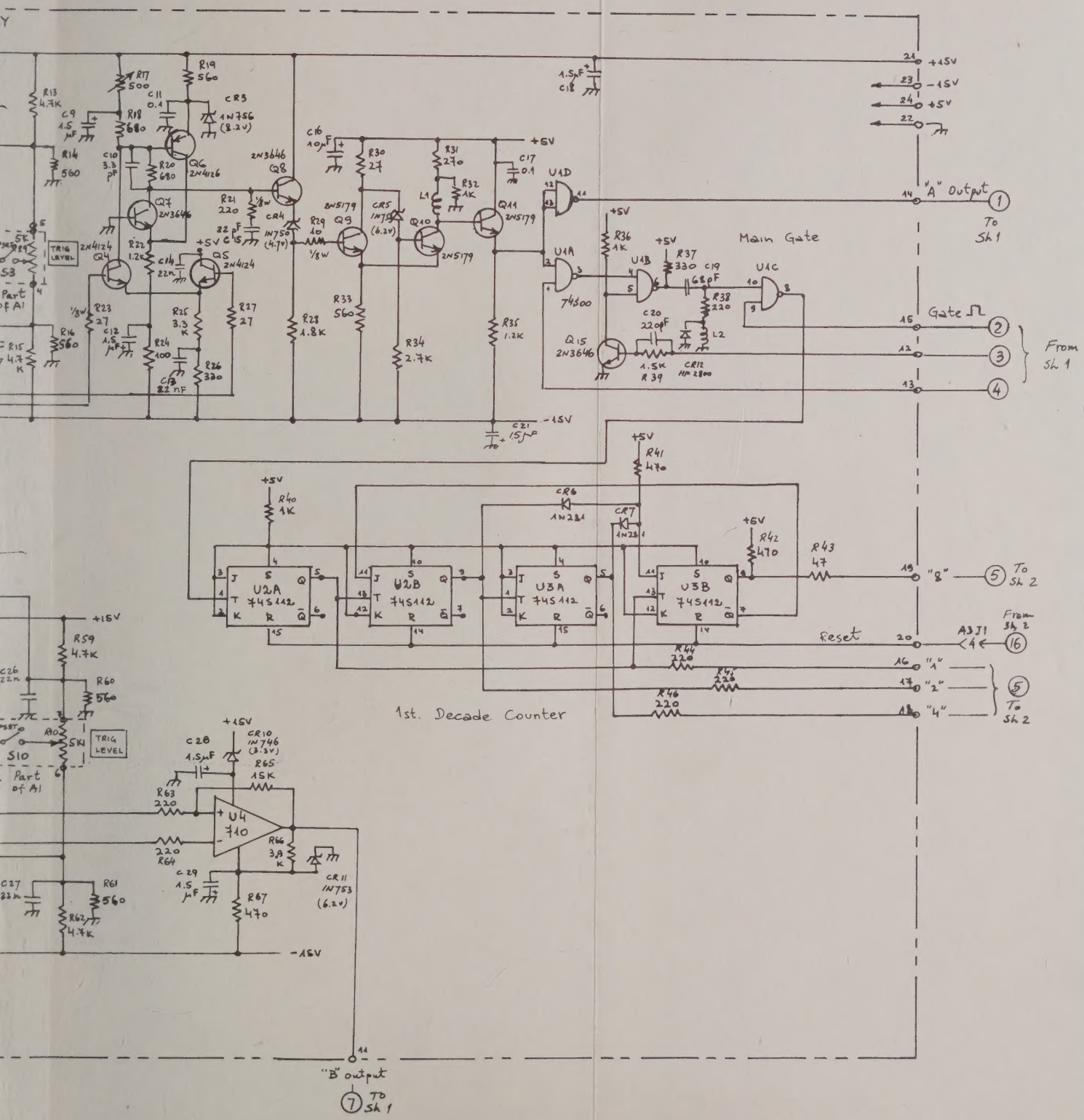


FIGURE 7-10. SCHEMATIC, FRONT PANEL A1 & INPUT CIRCUIT A5

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